UNIVERSITY OF THESSALY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

ECE196 – Digital Design
Fall Semester 2026-2027

Monday 19:00 – 22:00

Instructor: George Stamoulis

Office hours: Monday 11:00 – 14:00

Συγγράμματα:

Digital Design by M. Morris Mano.
Lecture notes.

Επιπλέον συγγράμματα:

Hachtel & Somenzi, Logic Synthesis and Verification Algorithms
Katz, Digital Design: From Gates to Intelligent Machines
Kohavi, Switching and Finite Automata Theory
De Micheli, Synthesis and Optimization of Digital Circuits

Grading:

8 homework sets	10%
Laboratory excercises	30%
Mid-term examinations	15% (5% + 10%)
Final examination	45%

A prerequisite for successful completion of the course is a grade of >2.9 in progress and >4.9 in laboratory exercises and the final exam.

Homework sets

Revision exercises:

8 sets of exercises will be given with 3 or 4 questions each. These exercises will be on the material covered and aim to understand basic concepts.

Laboratory exercises:

Laboratory exercises will be given starting from simple applications and ending with more complex structures.

Mid-terms – Final Examination

The first midterm will be given with the completion of the material of Boolean algebra. The second midterm will be given with the completion of the material concerning combined circuits. The final exam will be on the entire syllabus of the course.

Midterms and the final exam will be with open books and notes.

Course description

This course aims to convey the principles of the operation of digital circuits and to present basic structures used in logical design

Upon completion of the course, the goal is for the students to have acquired fluency in binary logic and the basic structures of logical design

The presentation of the material will follow the book by M. Morris Mano. The first part of the course will deal with combinational circuit design while the second will deal with sequential circuit design.

Week 1

Binary numbers, conversions between bases, complements
Addition-subtraction of binaries, signed numbers
Examples
Codes, BCD operations, binary logic, logic gates
Examples

1st homework set

Week 2

Boolean algebra, basic definitions, axiomatic definition
Two-value algebra, basic theorems
Logical functions, complement
Standard forms, conversions

1st homework set due
2nd homework set

Week 3

Logic gates, implementation of functions with gates
Minimization using Karnaugh maps

2nd homework set due
1st midterm

Week 4

Minimization using Karnaugh maps, don't-care conditions
Examples
Quine-McCluskey method, prime implicants
Examples

3rd homework set

Week 5

Implementations with NAND, NOR, AOI, OAI gates.
XOR gates.
Examples
Analysis, design of combinational circuits
Conversions between codes
Examples

3rd homework set due
4th homework set

Week 6

Binary Decision Diagrams
Examples
Adders, subtractors, multipliers, divisors, comparators

4th homework set due
5th homework set

Week 7

Decoders, encoders, priority encoders, multiplexers.
Design with decoders
Design with multiplexers
Review of combinational circuits

5th homework set due

Week 8

2nd midterm

Week 9

Key sequential elements, state diagram
State equations, input equations
Examples

Week 10

Analysis with D, T and JK flip-flop, Mealy and Moore models
State Coding and Minimization
Binary, Gray, one-hot, one-cold encodings
Design of sequential circuits, excitation tables
Flip-flop selection: D, T, JK
Examples

6η homework set

Week 11

Registers, shift registers, counters.
Unused States
Examples
RAM, ROM, PLA, finite memory circuits
Error detection and correction

6th homework set due

Week 12

Implication Table
Examples

7η homework set

Week 13

ASM Charts
Conversion to State Diagrams
Examples

7th homework set due
8η homework set

Week 14

Summary and final instructions

8th homework set due