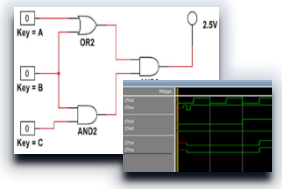
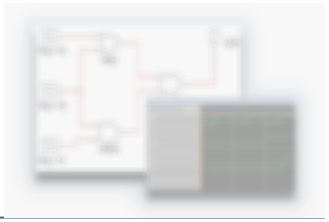


ECE119 – Ψηφιακή Σχεδίαση

Διδάσκοντες Εργαστηρίου: Δ. Καραμπερόπουλος
Δ. Γαρυφάλλου

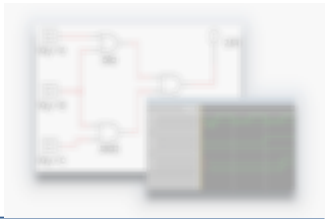
- Lab 9: Flip-Flops

Περιεχόμενα Εργαστηριακού Μαθήματος



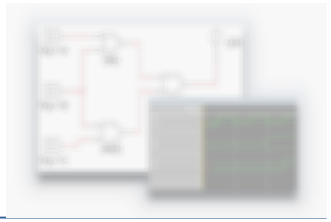
- Εισαγωγή
- Lab 1: Multisim Circuit Simulation and Basic Gates
- Lab 2: Truth Tables and Basic Logic Gates
- Lab 3: Logic Gates Explored and Boolean Algebra
- Lab 4: Karnaugh Maps
- Lab 5: Binary Conversion and Adders
- Lab 6: Encoders and Decoders
- Lab 7: Multiplexers and Demultiplexers
- Lab 8: Latches and Sequential Logic Circuits
- **Lab 9: Flip-Flops**
- Lab 10: Sequential Circuits - FSM

Flip-Flops



- In the previous lab, you were introduced to the concept of sequential logic circuits by examining **latches**.
- Particularly, you explored **D and SR latches**.
- In this lab, you will explore sequential logic circuits by focusing on **flip-flops**.
- **Flip flops** differ from latches in that they are **edge triggered**.
- **Latches** are **level sensitive** devices.
- Flip-flops can be constructed from latches.
- Together, flip-flops and latches are the building blocks of sequential logic circuits.

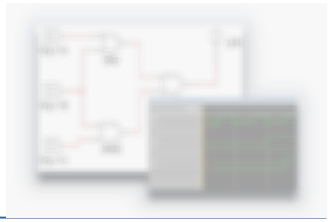
Learning Objectives



In this lab, students will:

- Become familiar with the basic behavior of **D, JK** and **T flip-flops**
- Explore variations of flip-flops in greater detail (i.e. master-slave relationships)
- Gain an awareness of the versatility of the DFF and its application in other circuits.

Expected Deliverables

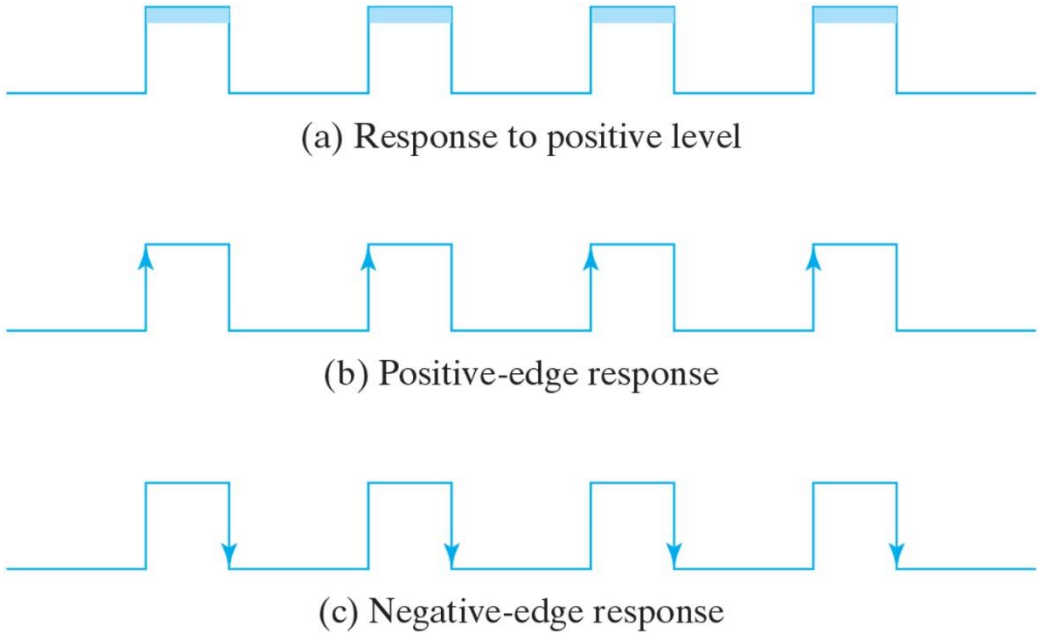


In this lab, you will collect the following deliverables:

- Flip-flop analysis
- Conclusion questions

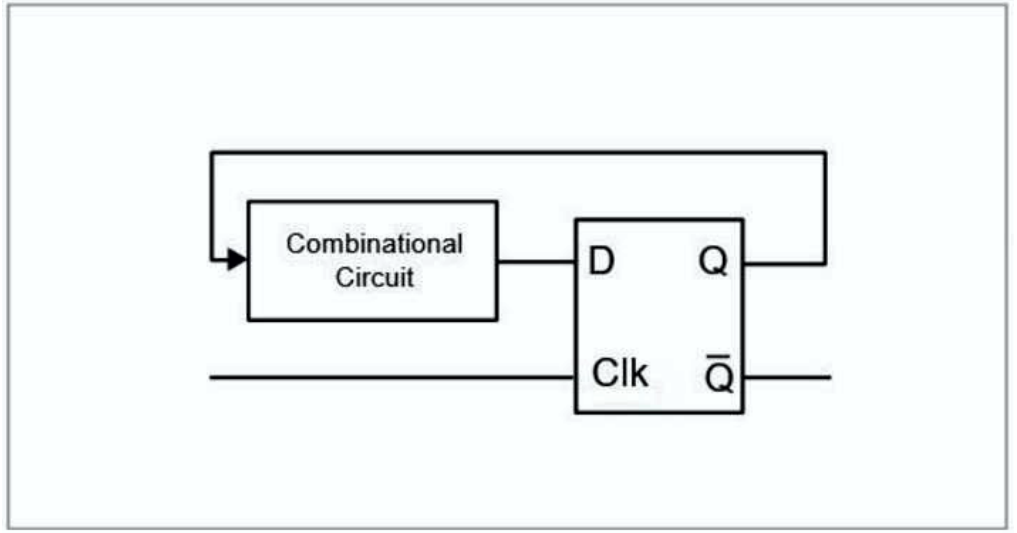
Flip-Flops

- Flip-flops are the fundamental building blocks of sequential circuits.
- They are **1-bit storage devices** that, unlike latches (which are level sensitive devices) are **edge-triggered**.
- Data gets stored into a flip-flop **at one of the edges** of the clock signal, i.e. when the clock input makes a transition from 0 to 1 or from 1 to 0.

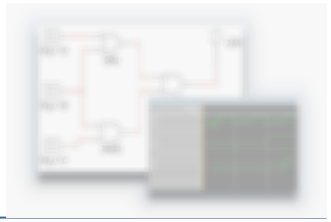


Latch Feedback

- The state transitions of the latches start in the moment the clock changes to 1 and can continue for the entire period while it is active.
- Because of this, the output of a latch cannot be applied through combinational circuits to the inputs of other latches triggered by the same clock signal.
- This fact represents a **serious drawback** when using latches as storage elements.
- **Flip-flops** overcome this problem by **triggering only during signal changes (edges)**.



D Flip-flops (DFFs)

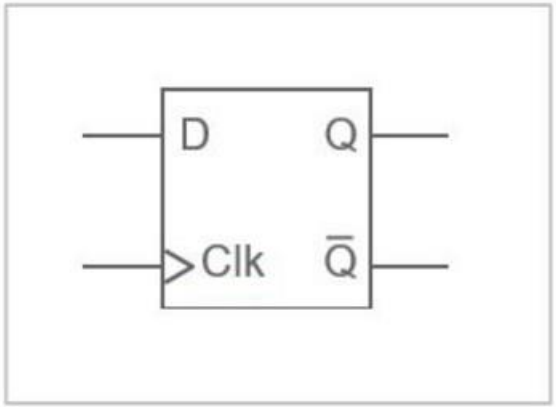


D flip-flops (DFFs) are very commonly used because they are perfectly suited for the construction of sequential circuits.

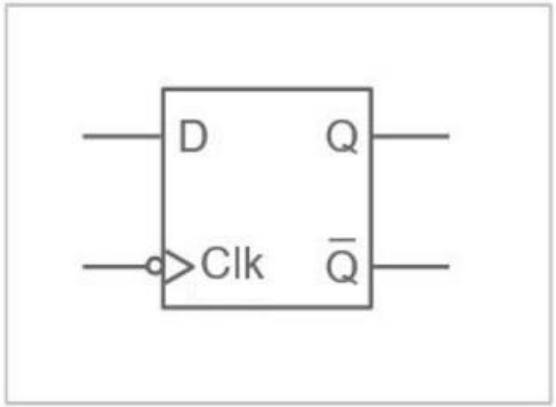
- If the DFF transfers the input to the output on the **rising edge** of the clock signal then it is said to be a positive-edge triggered D flip-flop or **positive-edge DFF**.
- If the DFF transfers the input to the output on the **falling edge** of the clock signal then it is said to be a negative-edge triggered D flip-flop or **negative-edge DFF**.

D Flip-flops (DFFs)

- This mode of operation is signaled through the use of a **circle** on the **clock input**. The image below shows the symbol for a positive-edge DFF (left) and a negative-edge DFF (right).
- For both DFF circuits shown below, the **small triangle** on the **clock input** indicates that the flip-flop will trigger only on one of the **clock edges**.
- The complemented output, Q is omitted in the graphical symbol when it is not needed.

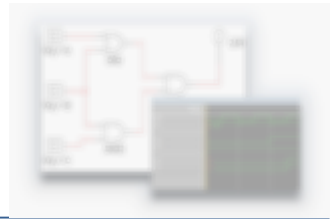


Positive edge DFF



negative edge DFF

D Flip-flops (DFFs)



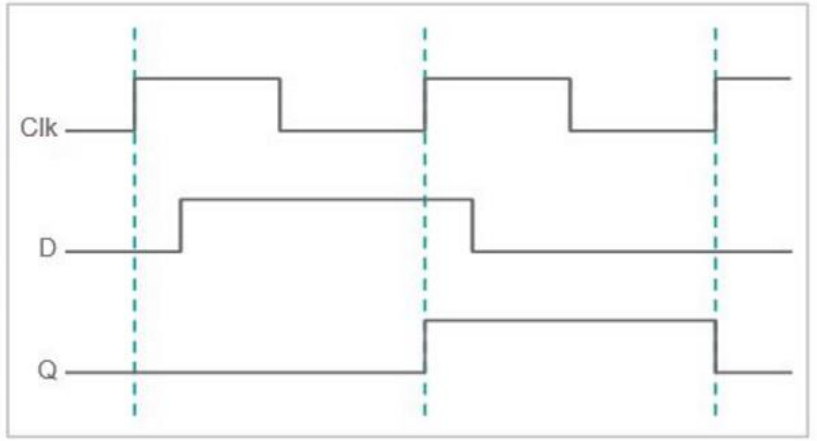
The operation of the **positive-triggered D flip-flop** is very simple:

- The output Q will go to the present state of the D input when the clock signal **changes from 0 to 1**
- The level present at the input will be stored in the flip-flop on the **rising transition** of the Clk signal.
- The figures below present the functionality of a positive-edge DFF:

Χαρακτηριστική εξίσωση

Q (t+1) = D

Clk	Q(t +1)
0	Q
1	Q
↑	D
↓	Q



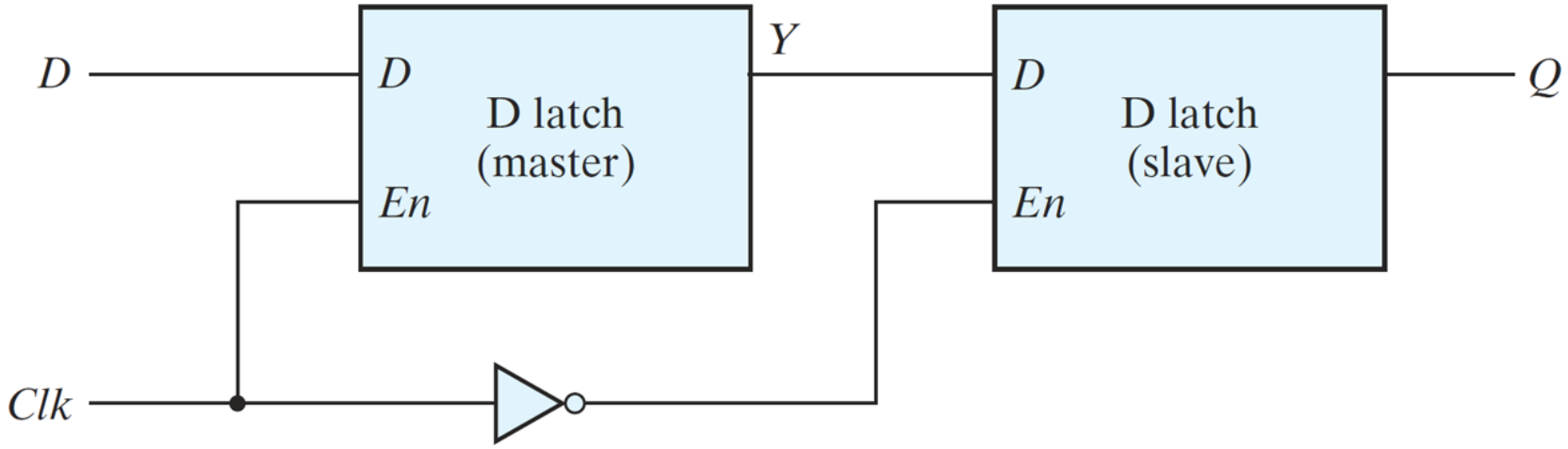
***D* Flip-Flop**

D	*Q*(*t* + 1)	
0	0	Reset
1	1	Set

D Flip-flops (DFFs)

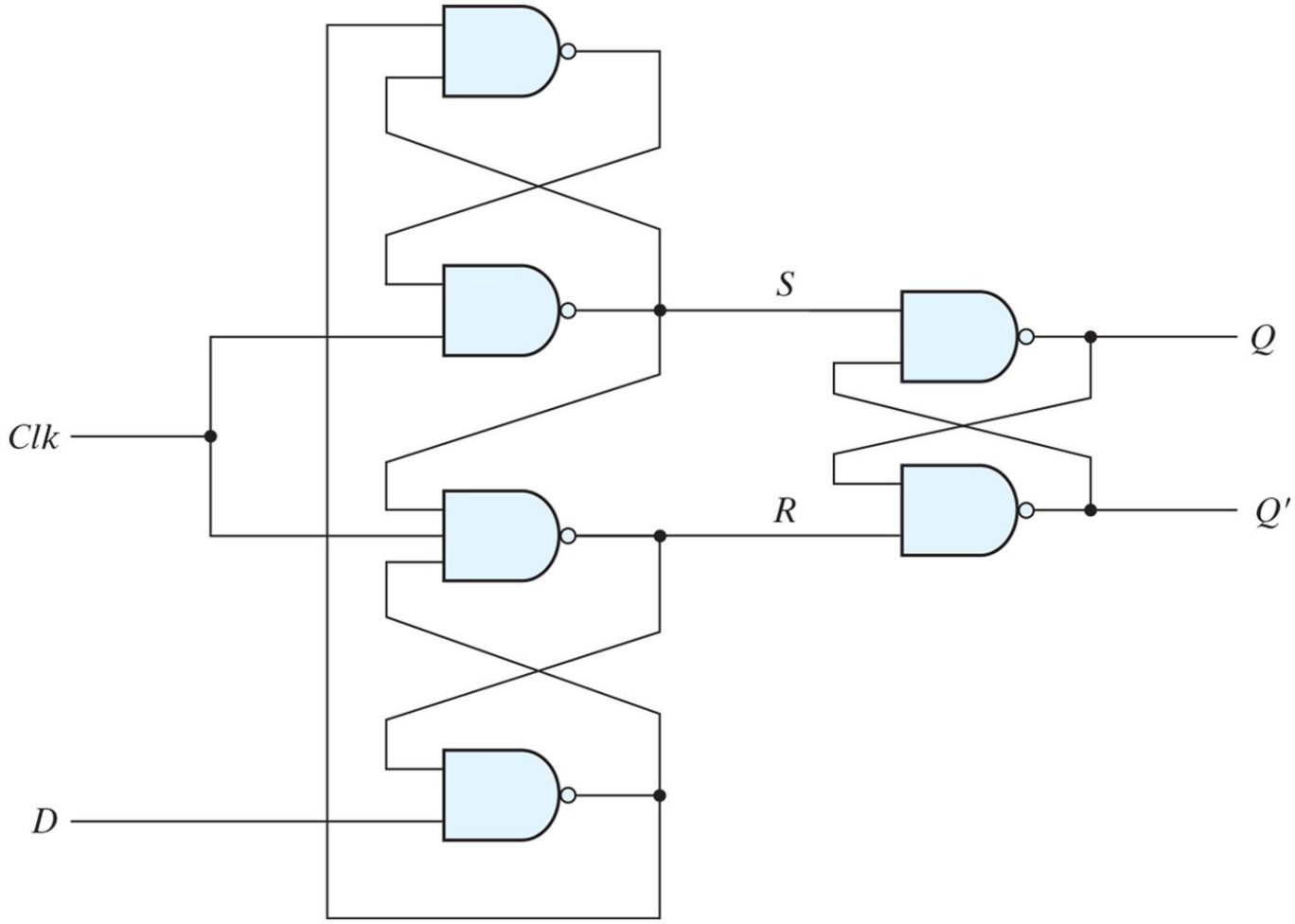
A flip-flop can be built using the following methods:

- Using **two D latches** arranged in a **master-slave** configuration, where one of them is transparent during one semi-period of the clock period and the other transparent during the other semi-period.

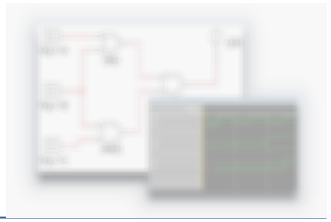


D Flip-flops (DFFs)

- Another circuit having the same operation, but implemented using fewer gates, can be built from **three SR latches**.



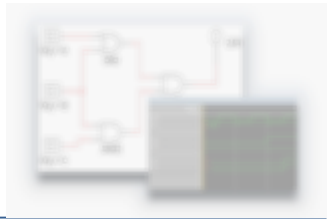
Flip-flops



The timing characteristics of flip-flops include:

- the **propagation delay (χρόνος καθυστέρησης διάδοσης)** from Clk to Q (the time needed for a value present on the input to reach the output when the clock changes from 0 to 1)
- the **setup time (χρόνος προετοιμασίας)**
- the **hold time (χρόνος συγκράτησης)**
- the **maximum frequency** that can be applied to the clock signal and still have correct operation

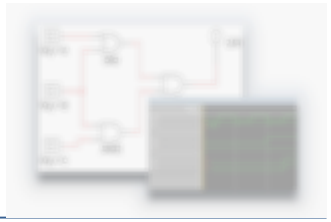
JK Flip-flop (JKFF)



Another type of flip-flop, one that is not as widely used as the DFF, but a more versatile one, is the **J K flip-flop (JKFF)**.

- The J K flip-flop is referred to as the **universal bi-stable** because it can easily behave like any one of the others.
- It has **two data inputs**, (**J and K**), a clock input, and two outputs (Q and $\bar{Q}$)
- **J acts as a SET** input and **K acts as a RESET** input.
- The output changes only on one of the **clock edges**.
- When both **J and K are 1**, the flip-flop **toggles** between opposite logic states each time the clock signal changes from 0 to 1 or from 1 to 0.
- This circuit is like the one of a gated SR latch with an edge detector, with the difference that the forbidden state (when both S and R are set to 1) is replaced by the toggle state.

JK Flip-flop (JKFF)



The golden rules of JKFFs are:

Χαρακτηριστική εξίσωση

$$Q(t+1) = J\,Q' + K'\,Q$$

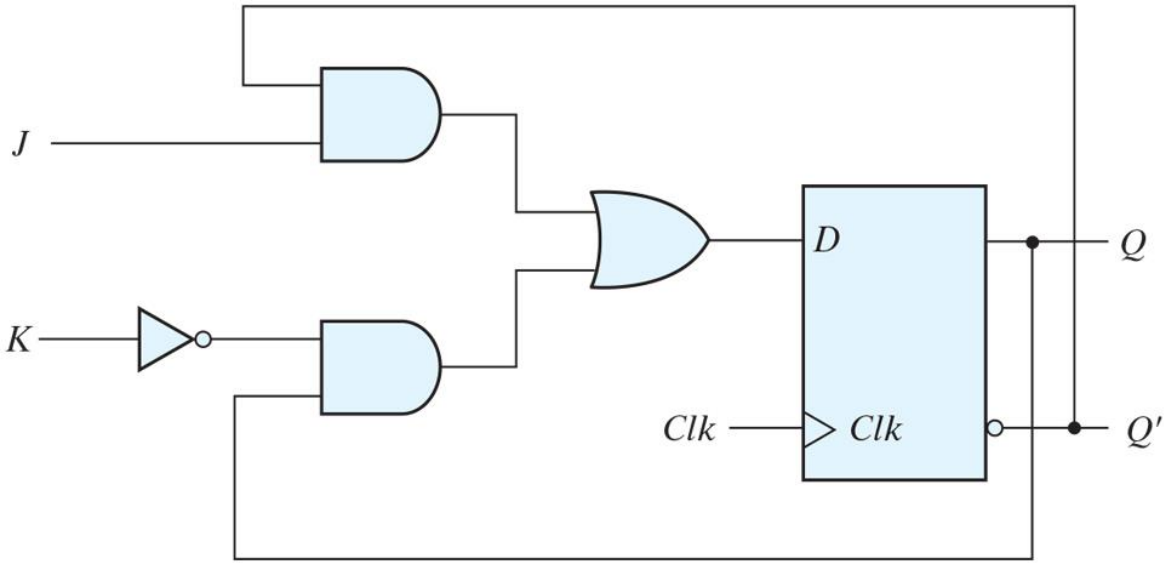
- If **J and K are 0**, **nothing happens**.
- If **J and K are 1**, **Q toggles**.
- If **J and K are different**, then **Q** is always the same as **J**.

***JK* Flip-Flop**

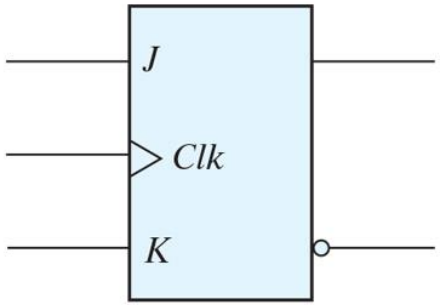
J	*K*	*Q*(*t* + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

JK Flip-flop (JKFF)

- The figures below present the way in which a J K flip-flop can be built using a DFF and logic gates. The graphical symbol of the JKFF is also shown below, and its operation is described by the characteristic table



(a) Circuit diagram



(b) Graphic symbol

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D = JQ’ + K’Q

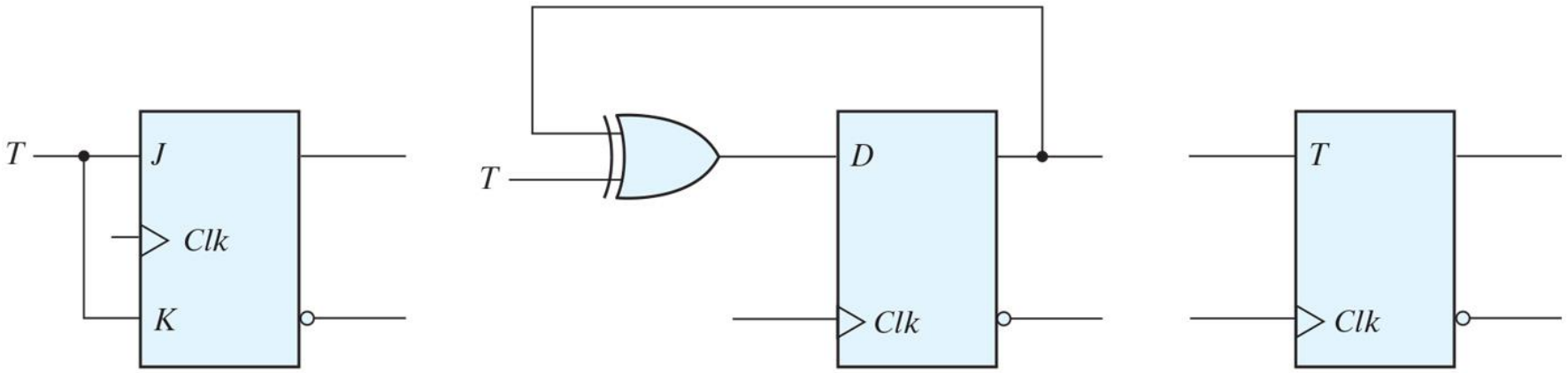
T flip-flop

A **T flip-flop** is a flip-flop whose **output toggles between 1 and 0** each applied clock pulse, when an input called T (from toggle) is active.

- The toggle mode of operation of a flip-flop is sometimes useful in synchronous circuits.
- It can be implemented using a DFF.

Χαρακτηριστική εξίσωση

$Q(t+1) = T \oplus Q = T\,Q' + T'Q$



(a) From *JK* flip-flop (b) From *D* flip-flop (c) Graphic symbol

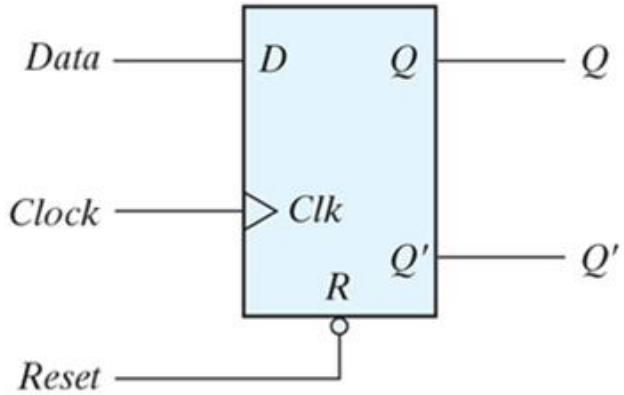
***T* Flip-Flop**

T	*Q*(*t* + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

Άμεσες είσοδοι

Ορισμένα flip flop διαθέτουν επιπλέον εισόδους, οι οποίες αποκαλούνται **ασύγχρονες είσοδοι**.

- Η είσοδος που θέτει το flip flop **στο 1** αποκαλείται είσοδος **άμεσης θέσης** (**preset** ή **direct set**)
- Η είσοδος που επαναφέρει το flip flop **στο 0** αποκαλείται είσοδος **άμεσου μηδενισμού** ή **άμεσης επαναφοράς** (**clear** ή **direct reset**).
- Ένα θετικά ακμοπυροδότητο D flip-flop με **ενεργή χαμηλά είσοδο ασύγχρονου μηδενισμού**, παρουσιάζεται παρακάτω.



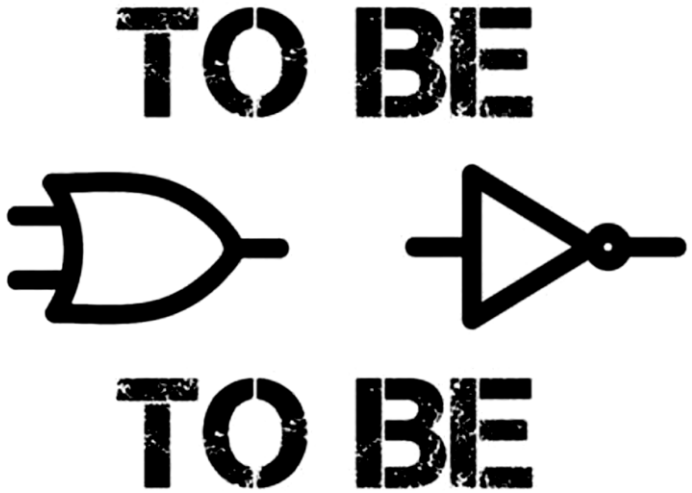
(b) Graphic symbol

R	Clk	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(c) Function table

Ευχαριστώ για την προσοχή σας!

- **Ερωτήσεις / Απορίες ;**



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