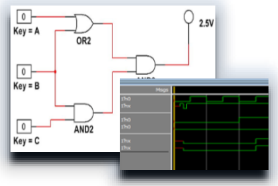
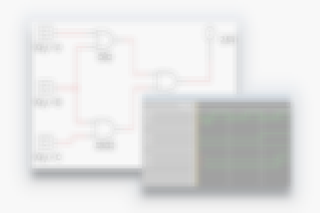


ECE119 – Ψηφιακή Σχεδίαση

Διδάσκοντες Εργαστηρίου: Δ. Καραμπερόπουλος
Α. Φεύγας

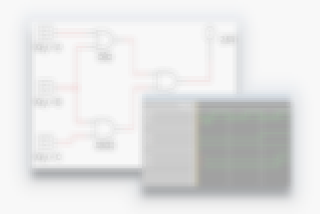
- Lab 6: Encoders and Decoders

Περιεχόμενα Εργαστηριακού Μαθήματος



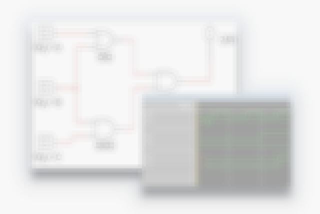
- Εισαγωγή
- Lab 1: Multisim Circuit Simulation and Basic Gates
- Lab 2: Truth Tables and Basic Logic Gates
- Lab 3: Logic Gates Explored and Boolean Algebra
- Lab 4: Karnaugh Maps
- Lab 5: Binary Conversion and Adders
- **Lab 6: Encoders and Decoders**
- Lab 7: Multiplexers and Demultiplexers
- Lab 8: Latches and Sequential Logic Circuits
- Lab 9: Flip-Flops
- Lab 10: Sequential Circuits – FSM (1^{o})
- Lab 11: Sequential Circuits – FSM (2^{o})

Encoders and Decoders



- In Lab 5, we learned that gates arranged to perform a specific function, such as binary addition, can be represented with a chip.
- Other applications of this concept include encoders and decoders.
- **Encoders** are logic circuits responsible for reducing the size of an input.
- **Decoders** preform the inverse operation, increasing the size of an input.
- In a previous lab, we learned what a seven-segment display is and in this lab we will explore how decoders apply to this electronic device.

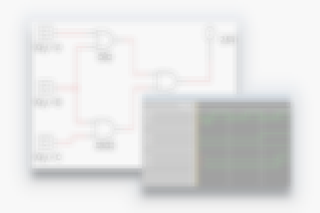
Learning Objectives



In this lab, students will:

- Explain how decoders works, specifically in an SSD
- Create a circuit with a BCD to Seven Segment Display Decoder and verify its truth table

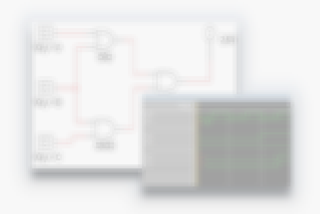
Expected Deliverables



In this lab, you will collect the following deliverables:

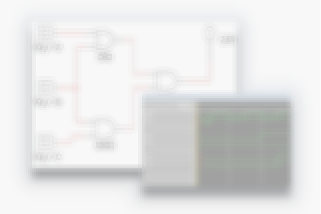
- Diagram of a BCD to 7 Segment Display Decoder
- Truth tables
- Conclusion questions

Decoders



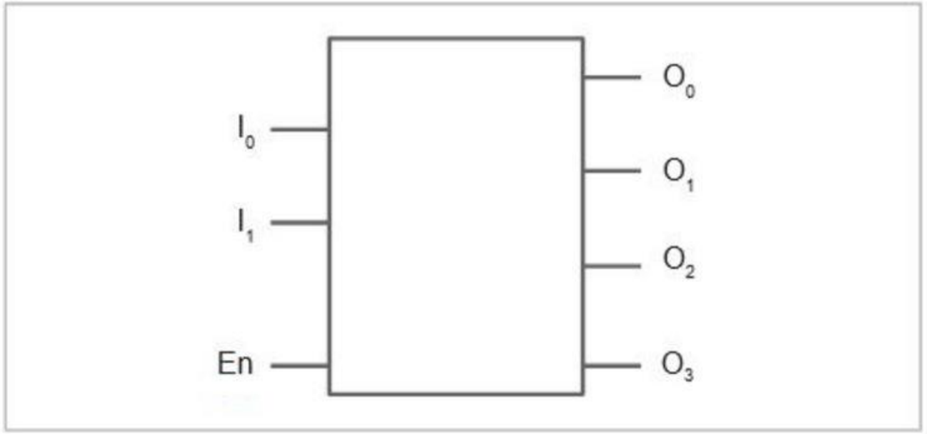
- The process of translating ambiguous information into something understood by a device receiving the data is called **decoding**.

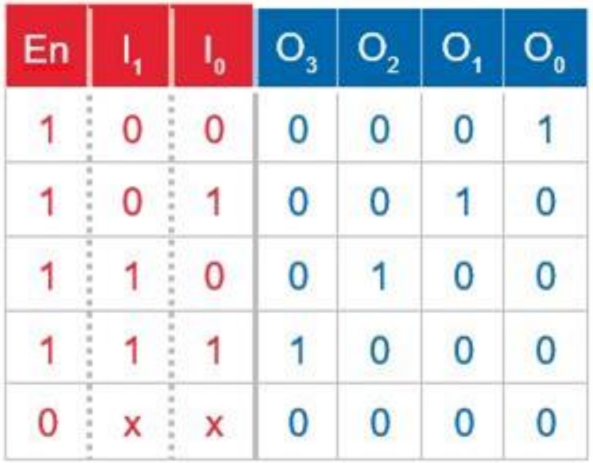
- Therefore, the resulting device is known as a **decoder**.



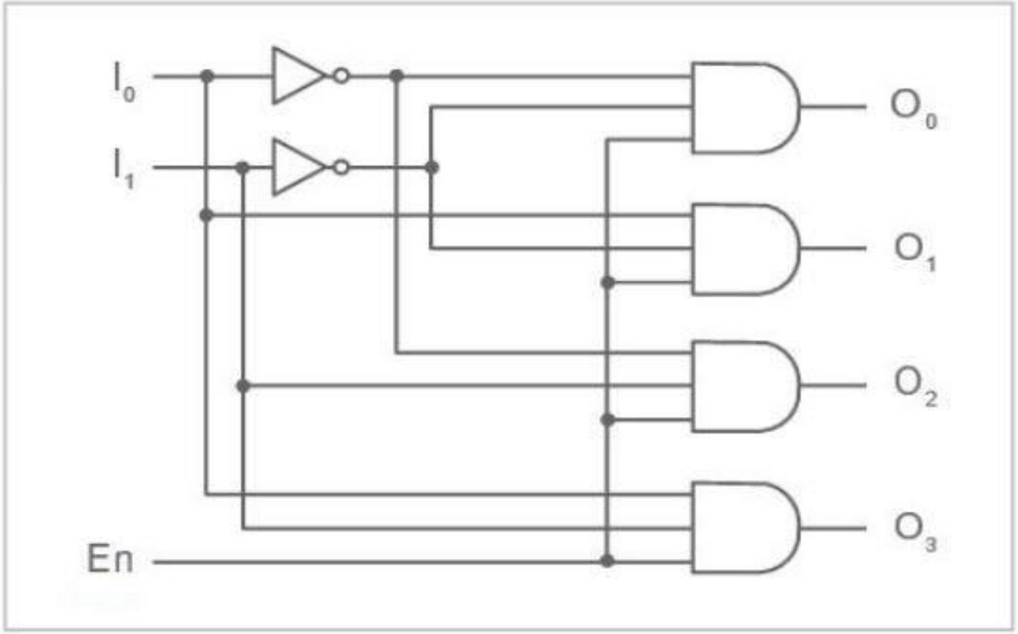
Decoders

- Let’s take the example of a 2 to 4 decoder enabled when the En signal is 1 (active-high):

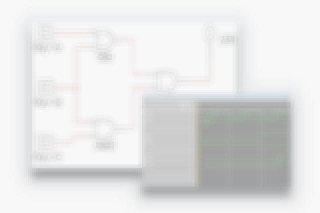




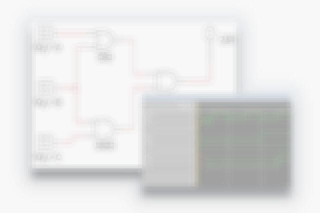
En	I_1	I_0	O_3	O_2	O_1	O_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0
0	x	x	0	0	0	0



Decoders

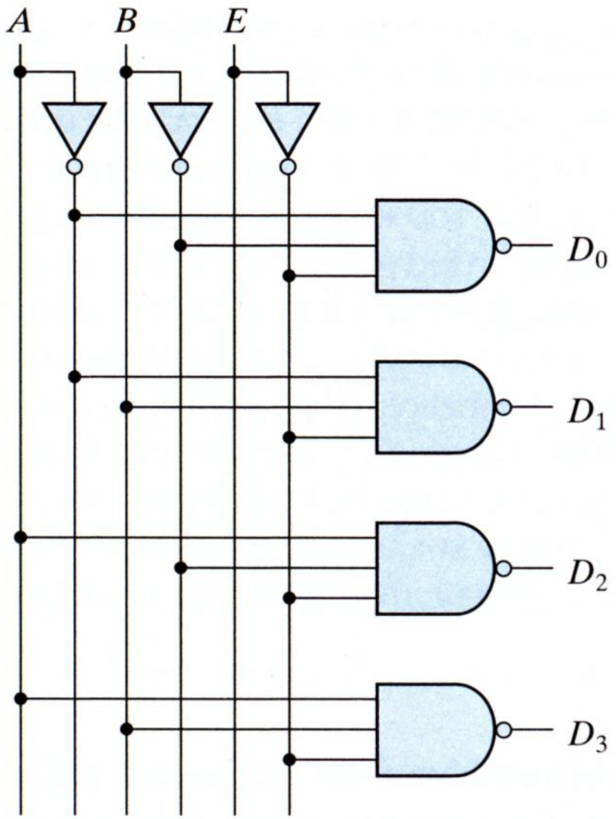


- **Decoders** take binary codes of n bits and generate 2^n outputs.
- The outputs of a binary decoder are said to be **one-hot encoded** because for any combination of the input signals there is only one output having the value 1.
- Decoders can include an **enable signal** for controlling the circuit operation.
- This enable signal can be **active-low** (meaning that the circuit will operate only when enable is 0) or **active-high** (the decoder is enabled when enable is 1).
- Decoders with enable inputs can be used for constructing larger decoders.
- One of the most important applications of decoders is memory access, where they are used for decoding the address of the rows in the memory blocks.



Decoders - 2x4 line decoder with enable input

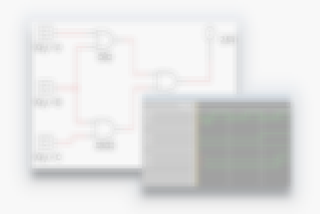
- And a 2 to 4 decoder enabled when the En signal is 0 (active-low):



E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

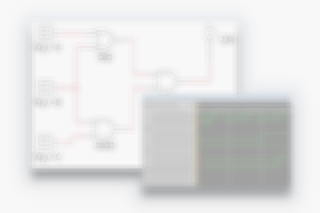
ΣΧΗΜΑ 4.19
Αποκωδικοποιητής 2 × 4 με είσοδο επίτρεψης

Encoders



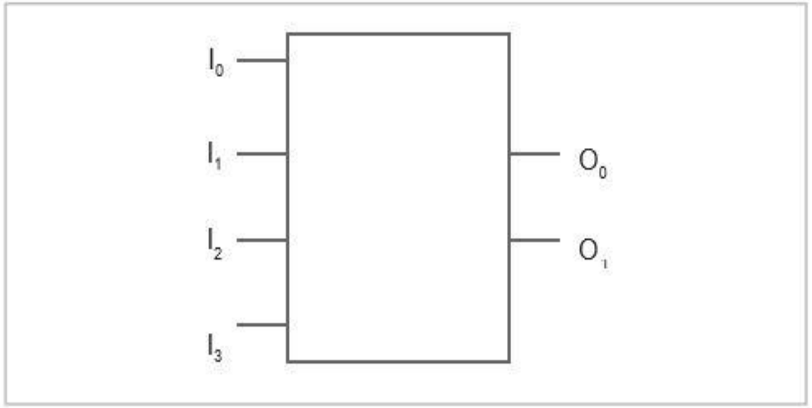
- **Encoders** are logic circuits that perform the opposite function of a decoder.

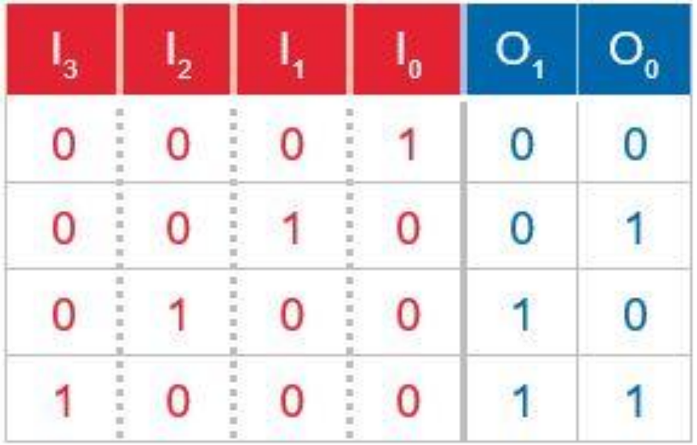
- Binary encoders encode information from 2^n input lines, producing an n-bit code.



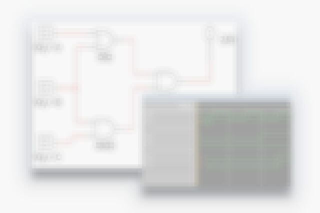
Encoders

- At any given time, **only one of the 2^n inputs can be 1**.
- Encoding is used for reducing the number of bits needed to represent information. They are often used in application such as data transmission and data storing.
- The graphical symbol of the 4 to 2 binary encoder is presented below. The cases in which more than one input is 1 are not shown in the truth table because they are treated as don’t care conditions.



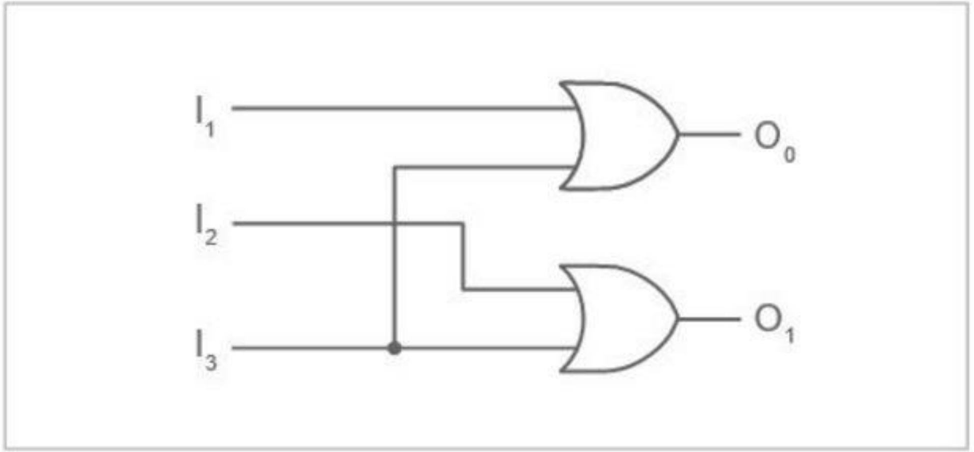


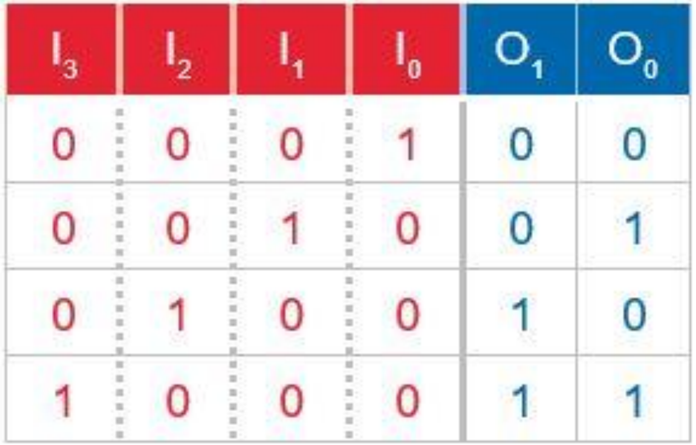
I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



Encoders

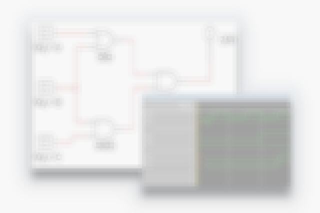
- It can be seen in the truth table that the output **O_1 is 1** when either **I_3 or I_2 is 1** and that the output **O_0 is 1** when either **I_3 or I_1 is 1**.
- It can also be seen that the input **I_0 can be ignored**
- The encoders presented so far are considered to have **one-hot encoded inputs**.



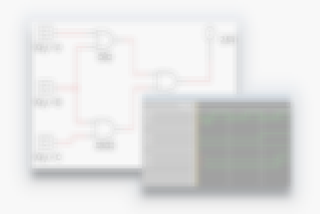


I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Priority encoders

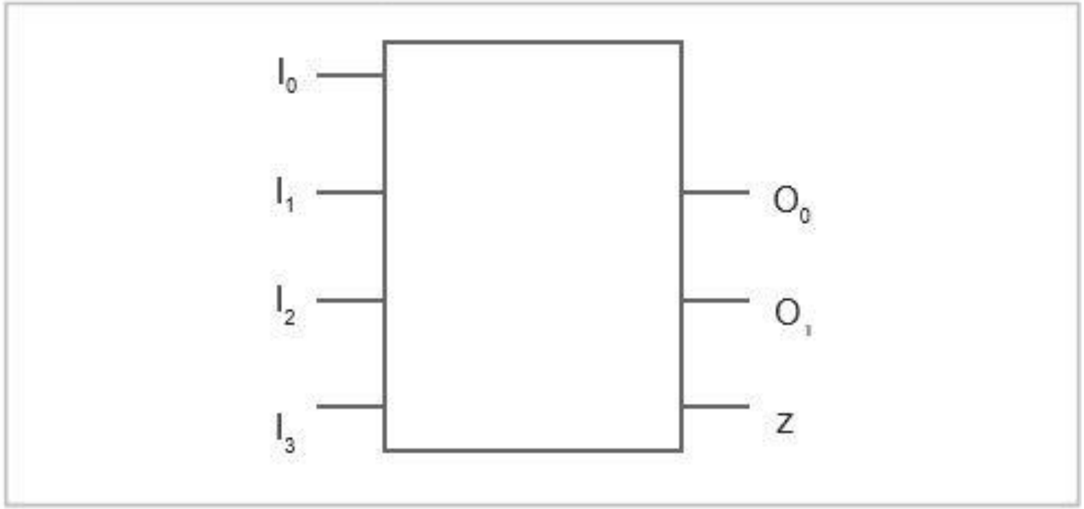


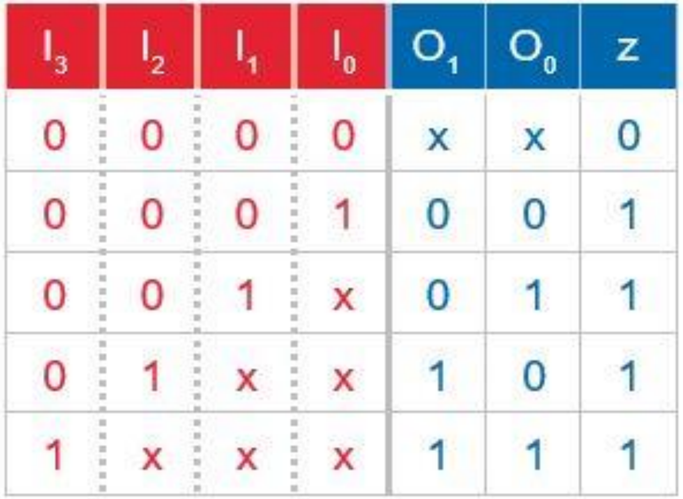
- **Priority encoders** are able to prioritize inputs
- This is important because regular encoders can generate the wrong output when there is more than one input present at logic level 1.
- This type of encoder has an **additional output, z**, which indicates the case in which none of the inputs is 1.



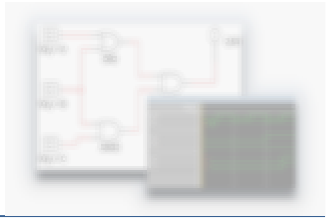
Priority encoders

- The graphical symbol of the priority encoder is presented below.
- The truth table describes the behavior of a 4-to-2 priority encoder.
- It can be seen on the last line of the truth table that if the input I_3 is 1, the outputs are all 1 and the values on the other inputs of the decode do not matter and are denoted by ‘x’.

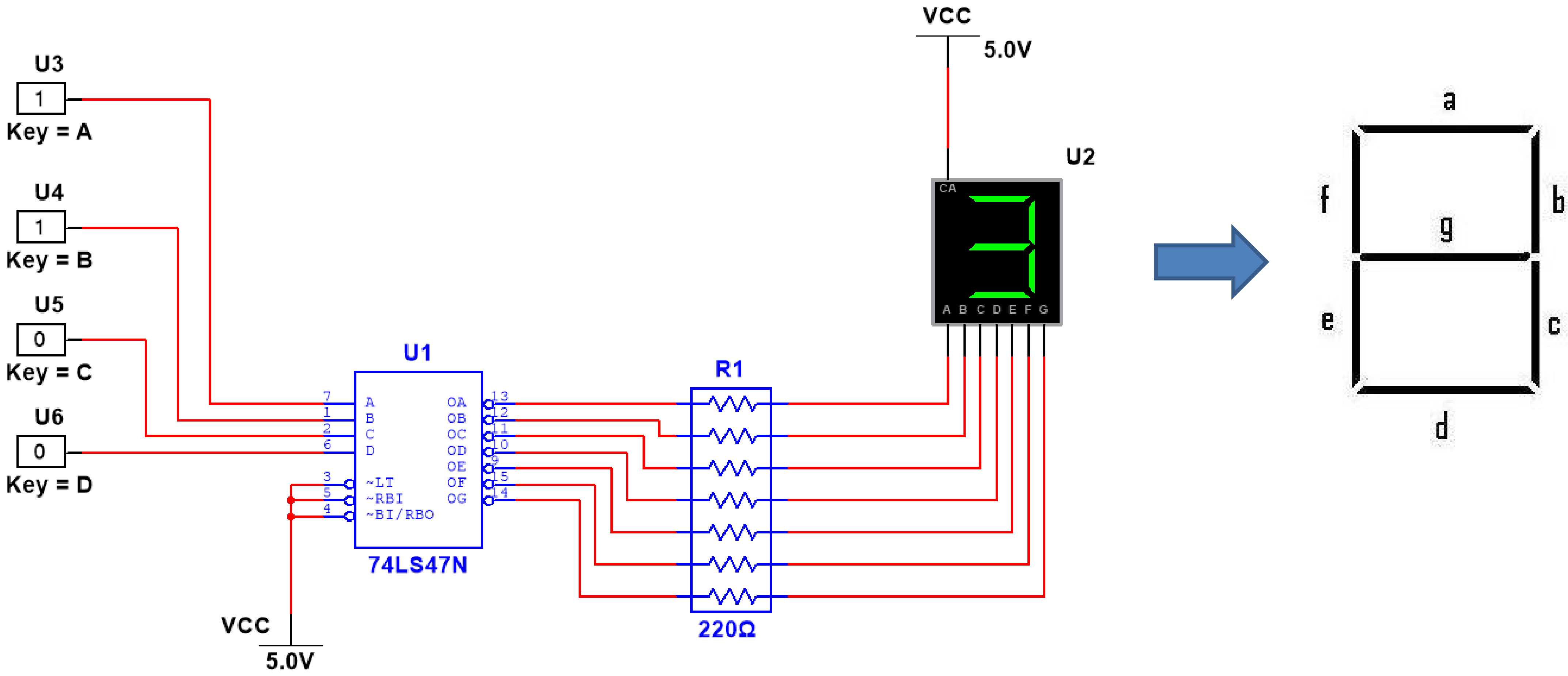


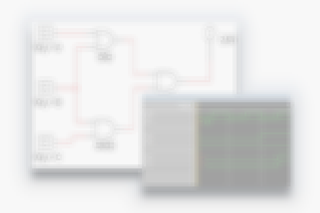


I_3	I_2	I_1	I_0	O_1	O_0	z
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1



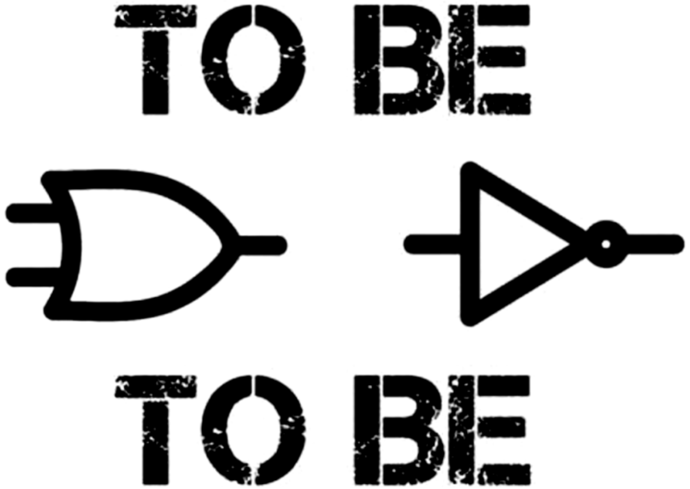
BCD to Seven Segment Display Decoder





Ευχαριστώ για την προσοχή σας!

- **Ερωτήσεις / Απορίες ;**



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