Hardware
Industrial IoT

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Contents

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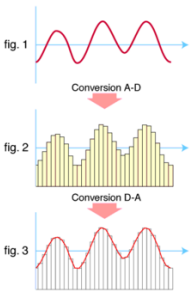
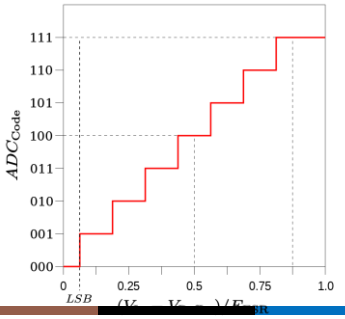
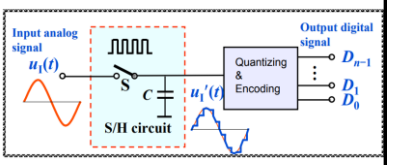
ADC vs DAC

- ADC (Analog to Digital Converter)
  - A circuit that transforms a signal from analog (continuous) to digital (discrete) form.
- DAC (Digital to Analog Converter)
  - A circuit that transforms from a digital form to an analog (Voltage, Current..)







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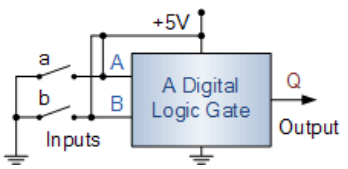
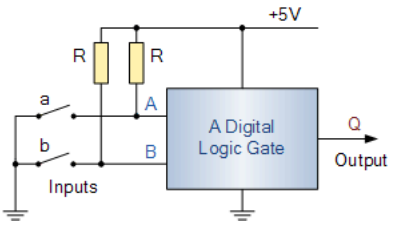
Pull-up and Pull-down Resistors

- Used to correctly bias the inputs of digital gates to stop them from floating about randomly when there is no input condition





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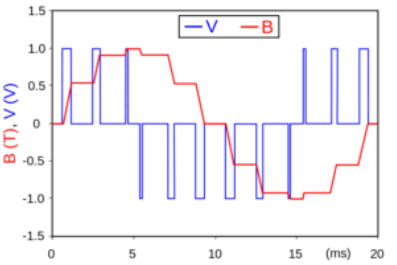
PWM (Pulse Width Modulation)

- Make a virtual analog signal, by combining multiple digital signal pulses with very low period time
- Used for motors and other devices that control mechanical parts



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Contents

- Analog Basics
  - ADC / DAC
  - Pull-up and Pull-Down Resistor
  - PWM
- **SoC Categories**
  - MCU
  - FPGA
  - SoC with Embedded FPGA
- Device Examples

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SoC Categories

- The most used core IP's on boards for IoT applications are:
  - Microcontroller Units (MCU)
  - Field Programmable Gate Arrays (FPGAs)
  - SoC with embedded FPGA (Zedboard)
- Each one is chosen according to the IoT application

MCUs

- Integrated circuits designed for specific operations in an embedded system
- Have standard hardware
- In order for the hardware components to function, embedded software is used to provide instructions for the system
- Embedded Software running: **firmware**
  - A specific class of computer software that provides the low-level control for a device's specific hardware
  - Developed specifically for this device
- Contain:
  - One or more processors (CPUs)
  - Memory (SD Card etc.)
  - input/output (I/O) peripherals

MCUs (continued)

- Advantages:
  - Lower cost of board and peripherals
  - Lower power consumption
- Disadvantages
  - Limited performance

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FPGAs

- Highly configurable, general purpose integrated systems filled with logic cells (small programmable digital building logic blocks)
- Contain:
  - An array of programmable logic blocks
    - Perform complex combinational functions
    - Simple logic gates
  - A hierarchy of configurable interconnects
    - Allow the blocks to be wired together in different configurations
  - Memory blocks
    - Flip-Flops
    - Complete blocks of memory

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FPGAs (continued)

- Advantages
  - Parallel execution
    - parallel multiple sensors measurements
  - Low complexity achieved by reusing modules on RTL level
  - Low power consumption
    - Etc machine learning applications
  - High performance
  - No need of delays before transmitting
    - because of parallel programming multiple data can be sent at the same time
    - Flexible configurable computing
- Disadvantages:
  - Hardware security issues
    - Exposed bitfile
    - Needs encryption
  - Needs more complex electronic design automation (EDA) software to configure interconnects efficiently

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MCU and FPGA differences

	MCUs	FPGAs
Learning curve	Learning curve with some cross-over in tools (e.g., the ever more widespread Eclipse IDE, shared languages).	Steeper learning curve.
Fixed/Floating point operations available	Fixed and floating point are widely available.	Mostly fixed point. Difficult to accommodate floating point.
Time-critical processing	Depends on requirements as to whether the MCU can accommodate. Limited reach.	Capable of sophisticated, time-critical signal processing with strict throughput and low latency requirements.
Portable design	Easier to port designs between MCUs with C/C++ language.	No universal design method that is portable.
Total Flexibility	Reprogramming software only.	Superior in software *and hardware* flexibility in customization. Dynamic reconfiguration is possible.
Development	Code changes can often be added after compilation like a patch, without re-compiling, for a facile development process.	Development iterations take longer with re-placing and rerouting required of FPGAs in the development process.
Tools	Open-source tools increasingly make the development process portable across platforms.	No portability across tools. Universal design methods are non-existent.

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SoC with Embedded FPGA

- Integrated circuits (chips) that integrate all or most components of a computer or other electronic system
- Contain:
  - Central Processing Unit (CPU)
  - Memory
  - Input/Output ports
  - Secondary storage
- May contain:
  - Digital, analog, mixed-signal
  - Radio frequency processing
- Optional peripherals on the board level:
  - Radio modems
  - GPU

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SoC with Embedded FPGA (continued)

- Advantages:
  - Easily adapted on customer's needs
  - Compute faster using parallelism
  - Minimized latency
  - Integration reduces part costs
  - Support diverse and evolving IoT gateway requirements
    - through flexible protocol switching/bridging and secure remote in-field upgrades
  - Extract maximum value from data analytics at the edge and in the data center
- Disadvantages
  - Complexity in product development
    - Careful of architecture development due to difficulty in power management (especially in IoT)
  - The cost of SoC with an embedded FPGA is more than using an MCU or an FPGA

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Contents

- Analog Basics
  - ADC / DAC
  - Pull-up and Pull-Down Resistor
  - PWM
- Gateway vs Sensor Device
- SoC Categories
  - MCU
  - FPGA
  - SoC with Embedded FPGA
- **Device Examples**

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MCUs – Available Boards (continued)

- NUCLEO – L152RE
  - Features:
    - STM32L152RET6 in LQFP64 package
    - ARM®32-bit Cortex®-M3 CPU
    - 32 MHz max CPU frequency
    - VDD from 1.65 V to 3.6 V
    - 512 KB Flash
    - 80 KB SRAM
    - 16 KB EEPROM
    - GPIO (51) with external interrupt capability
    - RTC
    - Timers (9)
    - I2C (2)
    - USART (5)
    - SPI (3)
    - USB 2.0 full speed
    - DAC (2)
    - LCD (1) 4x32 or 8x28
    - Operational Amplifiers (2)
    - Comparators

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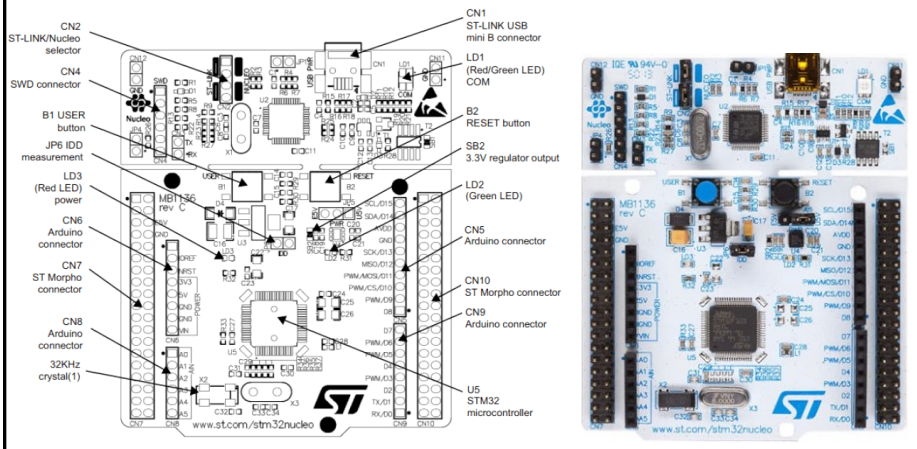
MCUs – Available Boards (continued)



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MCUs – Available Boards (continued)

- STM32WB55
  - Features:
    - A no crystal USB 2.0 interface
    - Up to 72 pins can be used as GPIO
      - 1 — USART
      - 1 — LPUART (Low Power UART)
      - 2 — SPI buses
      - 2 — I2C buses
    - Low power modes
    - Multiple ADC's (12 and 16 bit)
    - Support for capacitive touch sensors
    - An LCD driver
    - Embedded security options
    - 256 bytes to 1M of flash memory
    - Up to 256kB of RAM
    - Timers and comparators

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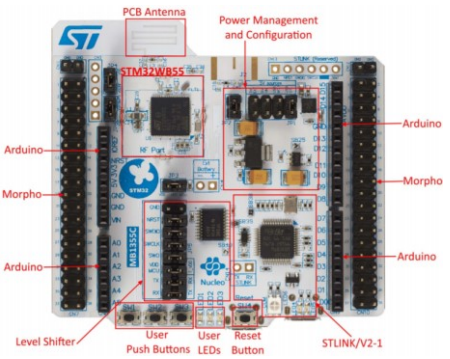
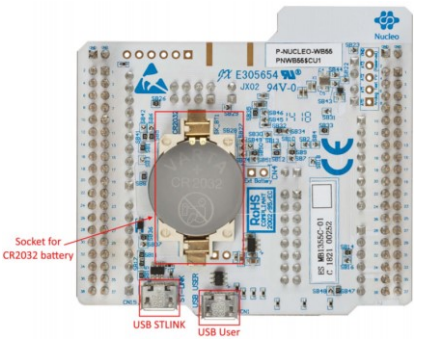
MCUs – Available Boards (continued)

- Nucleo-68 Board





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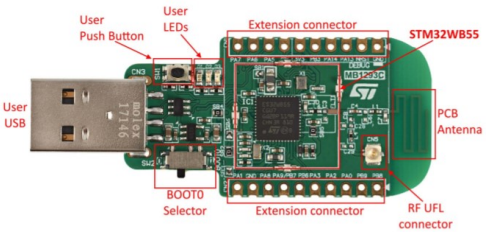
MCUs – Available Boards (continued)

- USB dongle Board



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FPGAs – Available Boards

- SPARTAN 3
  - Features:
    - Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
      - Densities up to 74,880 logic cells
    - SelectIO™ interface signaling
      - Up to 633 I/O pins
      - 622+ Mb/s data transfer rate per I/O
      - 18 single-ended signal standards
      - 8 differential I/O standards including LVDS, RSDS
      - Termination by Digitally Controlled Impedance
      - Signal swing ranging from 1.14V to 3.465V
      - Double Data Rate (DDR) support
      - DDR, DDR2 SDRAM support up to 333 Mb/s
    - Logic resources
      - Abundant logic cells with shift register capability
      - Wide, fast multiplexers
      - Fast look-ahead carry logic
      - Dedicated 18 x 18 multipliers
      - JTAG logic compatible with IEEE 1149.1/1532
    - SelectRAM™ hierarchical memory
      - Up to 1,872 Kbits of total block RAM
      - Up to 520 Kbits of total distributed RAM
    - Digital Clock Manager (up to four DCMs)
      - Clock skew elimination
      - Frequency synthesis
      - High resolution phase shifting
    - Eight global clock lines and abundant routing
    - Fully supported by Xilinx ISE® and WebPACK™ software development systems
    - MicroBlaze™ and PicoBlaze™ processor, PCI®, PCI Express® PIPE Endpoint, and other IP cores
    - Pb-free packaging options
    - Automotive Spartan-3 XA Family variant

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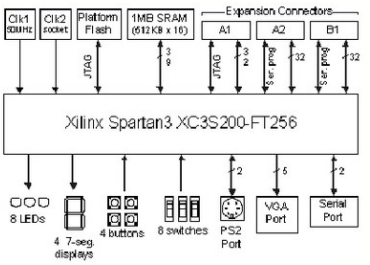
FPGAs – Available Boards



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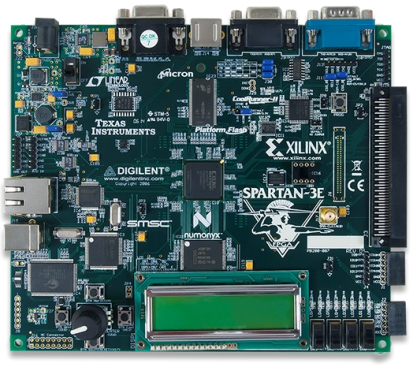
FPGAs – Available Boards

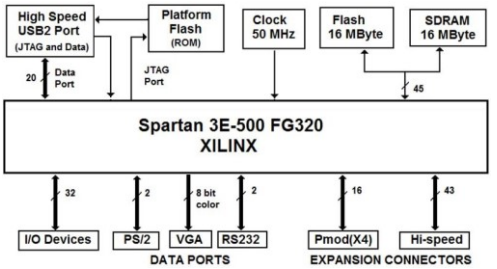
- SPARTAN 3E
  - Features
    - Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
    - Proven advanced 90-nanometer process technology
    - Multi-voltage, multi-standard SelectIO™ interface pins
      - Up to 376 I/O pins or 156 differential signal pairs
      - LVCMOS, LVTTL, HSTL, and SSTL single-ended signal standards
      - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
      - 622+ Mb/s data transfer rate per I/O
      - True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O
      - Enhanced Double Data Rate (DDR) support
      - DDR SDRAM support up to 333 Mb/s
    - Abundant, flexible logic resources
      - Densities up to 33,192 logic cells, including optional shift register or distributed RAM support
      - Efficient wide multiplexers, wide logic
      - Fast look-ahead carry logic
      - Enhanced 18 x 18 multipliers with optional pipeline
      - IEEE 1149.1/1532 JTAG programming/debug port
    - Hierarchical SelectRAM™ memory architecture
      - Up to 648 Kbits of fast block RAM
      - Up to 231 Kbits of efficient distributed RAM
    - Up to eight Digital Clock Managers (DCMs)
      - Clock skew elimination (delay locked loop)
      - Frequency synthesis, multiplication, division
      - High-resolution phase shifting
      - High-resolution phase shifting

FPGAs – Available Boards

- Eight global clocks plus eight additional clocks per each half of device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
- Complete Xilinx ISE® and WebPACK™ software
- MicroBlaze™ and PicoBlaze embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI support (66 MHz in some devices)
- Low-cost QFP and BGA packaging options
- Common footprints support easy density migration
- Pb-free packaging options
- XA Automotive version available

FPGAs – Available Boards





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FPGAs – Available Boards

- NEXYS A7
  - Features
    - Artix-7 FPGA
      - 15,850 Programmable logic slices, each with four 6-input LUTs and 8 flip-flops (*8,150 slices
      - 1,188 Kbits of fast block RAM (*600 Kbits)
      - Six clock management tiles, each with phase-locked loop (PLL)
      - 240 DSP slices (*120 DSPs)
      - Internal clock speeds exceeding 450 MHz
      - Dual-channel, 1 MSPS internal analog-digital converter (XADC)
    - Memory
      - 128MiB DDR2
      - Serial Flash
      - microSD card slot
    - Power
      - Powered from USB or any 4.5V-5.5V external power source
    - USB and Ethernet
      - 10/100 Ethernet PHY
      - USB-JTAG programming circuitry
      - USB-UART bridge
      - USB HID Host for mice, keyboards and memory sticks
    - Simple User Input/Output
      - 16 Switches
      - 16 LEDs
      - Two RGB LEDs
      - Two 4-digit 7-segment displays
    - Audio and Video
      - 12-bit VGA output
      - PWM audio output
      - PDM microphone
    - Additional Sensors
      - 3-axis accelerometer
      - Temperature sensor
    - Expansion Connectors
      - Pmod connector for XADC signals
      - Four Pmod connectors providing 32 total FPGA I/O

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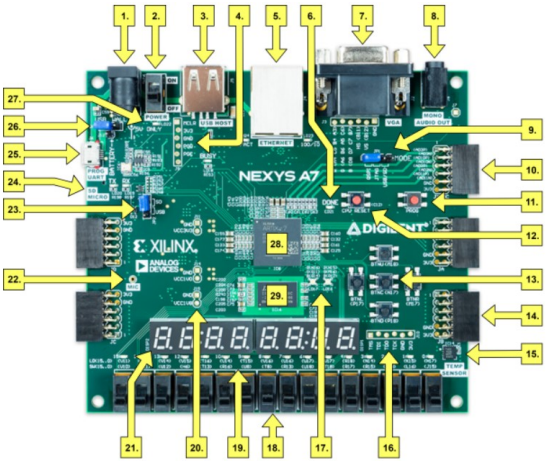
FPGAs – Available Boards



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FPGAs – Available Boards

Callout	Component Description	Callout	Component Description	Callout	Component Description
1	Power Jack	11	FPGA configuration reset button	21	Eight digit 7-segment display
2	Power switch	12	CPU reset button (for soft cores)	22	Microphone
3	USB Host Connector	13	Five pushbuttons	23	External configuration jumper (SD/USB)
4	PIC24 Programming port (factory use)	14	Pmod port(s)	24	MicroSD Card Slot
5	Ethernet connector	15	Temperature sensor	25	Shared UART/JTAG USB port
6	FPGA programming done led	16	JTAG port for (optional) external cable	26	Power select jumper and battery header
7	VGA connector	17	Tri-color (RGB) LEDS	27	Power-good LED
8	Audio connector	18	Slide switches (16)	28	Xilinx Artix-7 FPGA
9	Programming mode jumper	19	LEDs (16)	29	DDR2 memory
10	Analog Signal Pmod port (XDAC)	20	Power supply test point(s)		

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SoC with Embedded FPGA (continued)

- Zedboard (Zync 7000)
  - Features
    - Processing system (PS)
      - Application Processor Unit (APU)
        - 2.5 DMIPS/MHz per CPU
        - CPU frequency: Up to 1 GHz
        - Coherent multiprocessor support
        - ARMv7-A architecture
          - TrustZone® security
          - Thumb®-2 instruction set
        - Jazelle® RCT execution Environment Architecture
        - NEON™ media-processing engine
        - Single and double precision Vector Floating Point Unit (VFPU)
        - CoreSight™ and Program Trace Macrocell (PTM)
        - Timer and Interrupts
          - Three watchdog timers
          - One global timer
          - Two triple-timer counters
      - Caches
        - 32 KB Level 1 4-way set-associative instruction and data caches (independent for each CPU)
        - 512 KB 8-way set-associative Level 2 cache (shared between the CPUs)
        - Byte-parity support
      - On-Chip Memory
        - On-chip boot ROM
        - 256 KB on-chip RAM (OCM)
        - Byte-parity support
      - External Memory Interfaces
        - Multiprotocol dynamic memory controller
        - 16-bit or 32-bit interfaces to DDR3, DDR3L, DDR2, or LPDDR2 memories
        - ECC support in 16-bit mode
        - 1GB of address space using single rank of 8-, 16-, or 32-bit-wide memories
        - Static memory interfaces
          - 8-bit SRAM data bus with up to 64 MB support
          - Parallel NOR flash support
          - ONFI1.0 NAND flash support (1-bit ECC)
          - 1-bit SPI, 2-bit SPI, 4-bit SPI (quad-SPI), or two quad-SPI (8-bit) serial NOR flash
      - 8-Channel DMA Controller
        - Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and scatter-gather transaction support

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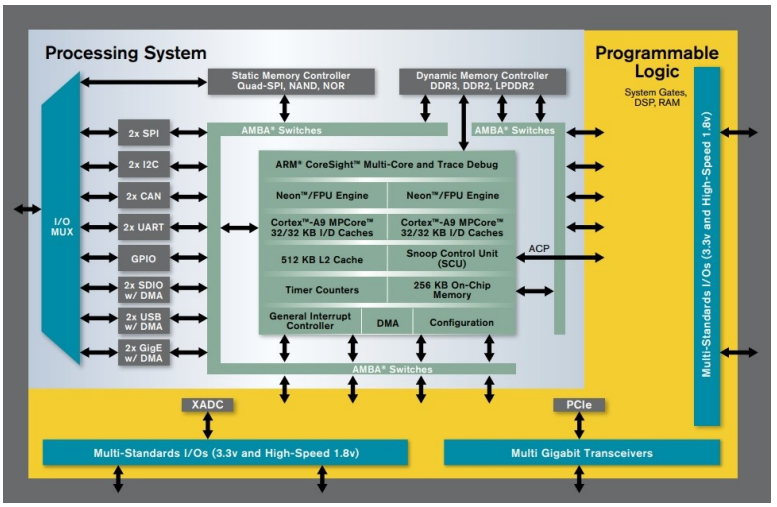
SoC with Embedded FPGA (continued)

- I/O Peripherals and Interfaces
  - Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE Std 802.3 and IEEE Std 1588 revision 2.0 support
    - Scatter-gather DMA capability
    - Recognition of 1588 rev. 2 PTP frames
    - GMII, RGMII, and SGMII interfaces
  - Two USB 2.0 OTG peripherals, each supporting up to 12 Endpoints
    - USB 2.0 compliant device IP core
    - Supports on-the-go, high-speed, full-speed, and low-speed modes
    - Intel EHCI compliant USB host
    - 8-bit ULPI external PHY interface
  - Two full CAN 2.0B compliant CAN bus interfaces
    - CAN 2.0-A and CAN 2.0-B and ISO 118981-1 standard compliant
    - External PHY interface
  - Two SD/SDIO 2.0/MMC3.31 compliant controllers
  - Two full-duplex SPI ports with three peripheral chip selects
  - Two high-speed UARTs (up to 1 Mb/s)
  - GPIO with four 32-bit banks, of which up to 54 bits can be used with the PS I/O (one bank of 32b and one bank of 22b) and up to 64 bits (up to two banks of 32b) connected to the Programmable Logic
  - Up to 54 flexible multiplexed I/O (MIO) for peripheral pin assignments
- Interconnect
  - High-bandwidth connectivity within PS and between PS and PL
  - ARM AMBA® AXI based
  - QoS support on critical masters for latency and bandwidth control

SoC with Embedded FPGA (continued)

- Programmable Logic
  - Configurable Logic Blocks (CLB)
    - Look-up tanles (LUT)
    - Flip-Flops
    - Cascadeable adders
  - 36 KB Block RAM
    - True Dual-Port
    - Up to 72 bits wide
    - Configurable as dual 18 Kb block RAM
  - DSP Blocks
    - 18 x 25 signed multiply
    - 48-bit adder/accumulator
    - 25-bit pre-adder
  - Two 12-Bit Analog-to-Digital Converters
    - On-chip voltage and temperature sensing
    - Up to 17 external differential input channels
    - One million samples per second maximum conversion rate
  - Programmable I/O Blocks
    - Supports LVCMOS, LVDS, and SSTL
    - 1.2V to 3.3V I/O
    - Programmable I/O delay and SerDes
  - JTAG Boundary Scan
    - IEEE Std 1149.1 Compatible Test Interface
  - PCI Express® Block
    - Supports Root complex and End Point configurations
    - Supports up to Gen2 speeds
    - Supports up to 8 lanes
  - Serial Transceivers
    - Up to 16 receivers and transmitters
    - Supports up to 12.5 Gb/s data rates

SoC with Embedded FPGA (continued)



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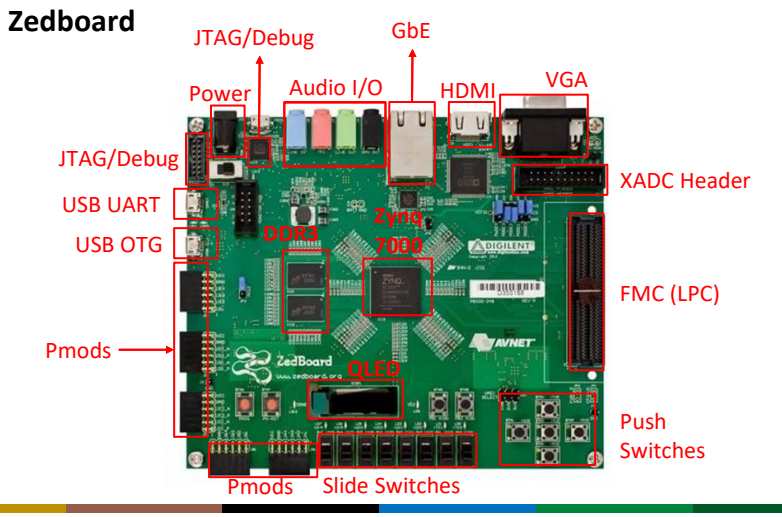
SoC with Embedded FPGA (continued)



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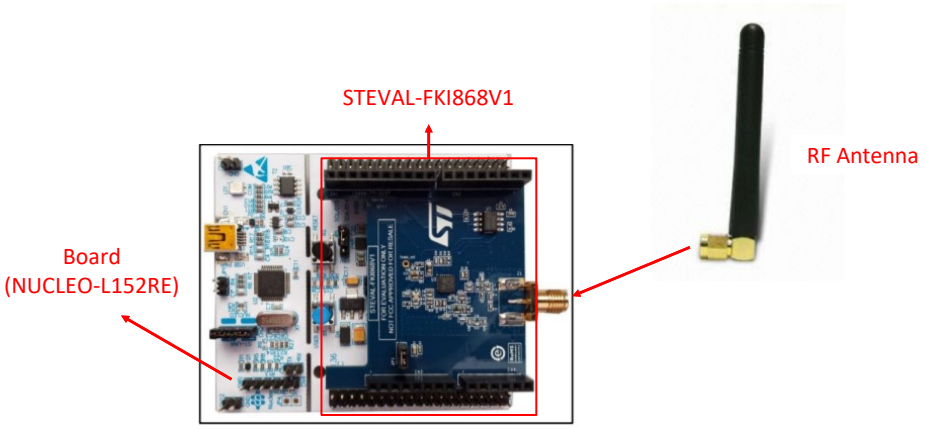
Available RF Components (continued)



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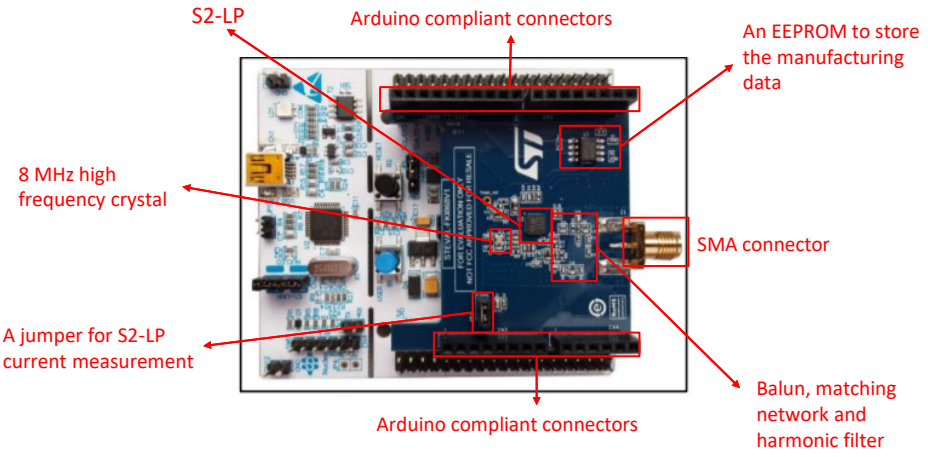
Available RF Components (continued)



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Sensors

- Modules that detect events or changes in their environment and send the information to other electronics (microcontrollers, computer processors etc.)
- There are two types of sensors
  - Digital sensors
    - Electronic or electrochemical sensors where data is digitally converted and transmitted
    - Often used for analytical measurements
    - Tend to replace analog sensors
  - Analog sensors
    - devices that produce analog output in correspondence to the quantity being calculated
    - Observe the change measured in external factors

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Available sensors

- Flame: KY-026
- Joystick: KY-023
- RGB LED: KY-016
- Heartbeat: KY-039
- Light Cup: KY-027
- Hall Magnetic: KY – 003
- Relay sensor: KY-019
- Linear hall: KY-024
- SMD RGB: KY-009
- Digital temp: KY-028
- Tilt Switch: KY-017
- TEMP 18B20: KY-001
- Big sound: KY-037
- Touch: KY-036
- Two-color LED: KY-011
- Laser emit: KY-008
- Ball switch: KY-020
- Analog temp: KY-013
- Small sound: KY-038
- 7 Color Flash: KY-034

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Available sensors (continued)

- Button: KY-004
- Photoresistor: KY-018
- IR emission: KY-005
- Tracking: KY-033
- Buzzer: KY-012
- Reed switch: KY-025
- Shock: KY-002
- Temp and humidity: KY-015
- IR receiver: KY-022
- Two-color: KY-029
- Passive buzzer: KY-006
- Mini reed: KY-021
- Rotary encoders: KY-040
- Analog hall: KY-035
- Tap module: KY-031
- Light blocking: KY-010
- Avoid: KY-032

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