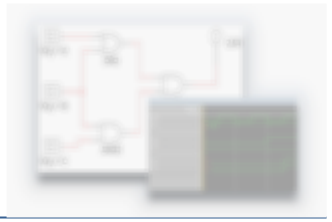


ECE119 – Ψηφιακή Σχεδίαση

Διδάσκοντες Εργαστηρίου: Δ. Καραμπερόπουλος
Α. Φεύγας
Μ. Πανταζή

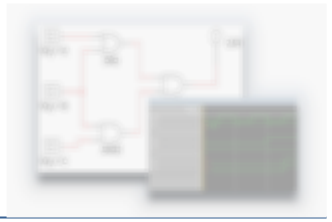
- Lab 7: Multiplexers and Demultiplexers

Περιεχόμενα Εργαστηριακού Μαθήματος



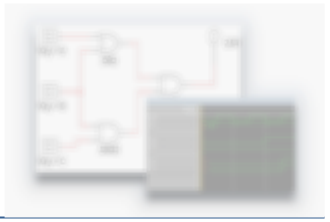
- Εισαγωγή
- Lab 1: Multisim Circuit Simulation and Basic Gates
- Lab 2: Truth Tables and Basic Logic Gates
- Lab 3: Logic Gates Explored and Boolean Algebra
- Lab 4: Karnaugh Maps
- Lab 5: Binary Conversion and Adders
- Lab 6: Encoders and Decoders
- **Lab 7: Multiplexers and Demultiplexers**
- Lab 8: Latches and Sequential Logic Circuits
- Lab 9: Flip-Flops
- Lab 10: Sequential Circuits – FSM (1ο)
- Lab 11: Sequential Circuits – FSM (2ο)

Multiplexers and Demultiplexers



- A **multiplexer** (MUX) is a combinational logic circuit that selects one of several data inputs and forwards its value to a single output.
- A **demultiplexer** (DEMUX) is a combinational logic circuit that routes a single data input to one of several outputs.
- Both circuits use **select lines** to determine which input or output is selected.
- Multiplexers and demultiplexers can be implemented using logic gates or integrated circuits.
- In this lab, we will examine their operation using logic diagrams, truth tables, and circuit simulations.

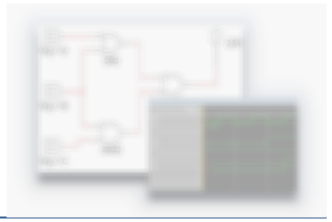
Learning Objectives



In this lab, students will:

- Explain the operation of multiplexers and demultiplexers.
- Distinguish between multiplexers, demultiplexers, encoders, and decoders.
- Understand how select lines determine the routing of data.
- Analyze 2-to-1 and 4-to-1 multiplexers using truth tables and Boolean expressions.
- Analyze a 1-to-4 demultiplexer using logic gates and Boolean expressions.
- Build and simulate multiplexer and demultiplexer circuits.

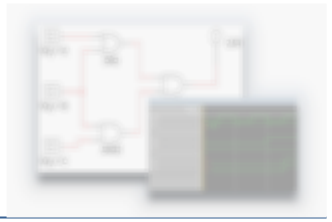
Expected Deliverables



In this lab, you will collect the following deliverables:

- Sum-of-Products Boolean functions for the 2-to-1 Multiplexer and the 1-to-4 Demultiplexer.
- Multisim circuit files.
- Verilog files.
- Screenshot of the simulation waveforms.
- Observations of demultiplexer behavior.
- Answers to the Check Your Understanding and Conclusion questions.

Multiplexers (MUX)



A **multiplexer** is a combinational logic circuit that selects one of several data inputs and forwards its value to a single output.

- The selected input is determined by the binary value of the **select lines**.
- A standard MUX with **s select lines** can select among **2^s data inputs**.

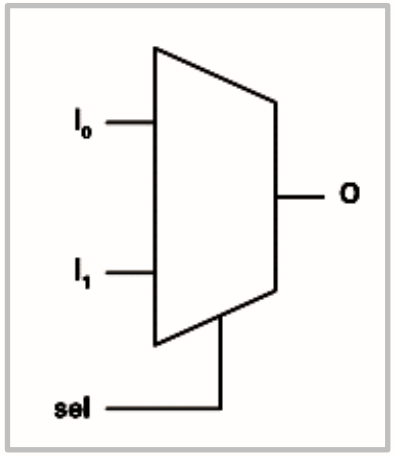
For example:
2-to-1 MUX: 1 select line
4-to-1 MUX: 2 select lines
8-to-1 MUX: 3 select lines.

- Common applications:
  Data routing and selection
  Selection of operands or operations in digital systems
  Parallel-to-serial data selection
  Selection of digital waveforms or signals

Multiplexers (MUX)

- The simplest circuit is the 2-to-1 multiplexer, with the graphical symbol presented in the leftmost figure.
- Its functionality is described by the corresponding truth table.
- The multiplexer below is only 1-bit wide because each data input and the output are one bit wide.

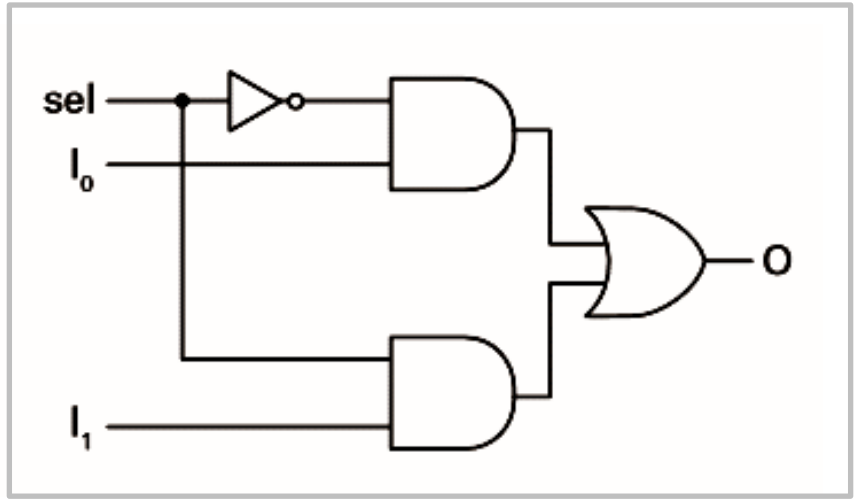
2-to-1 MUX



sel	I_0	I_1	O
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

summarized

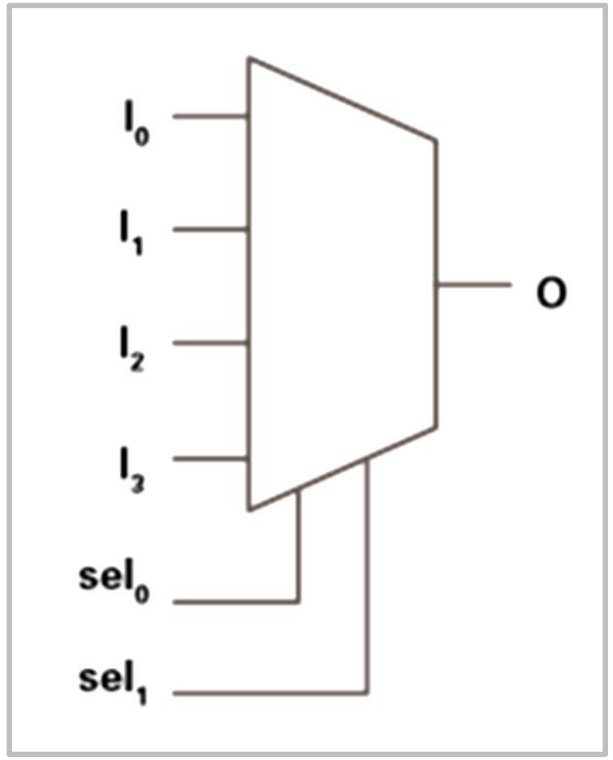
sel	O
0	I_0
1	I_1



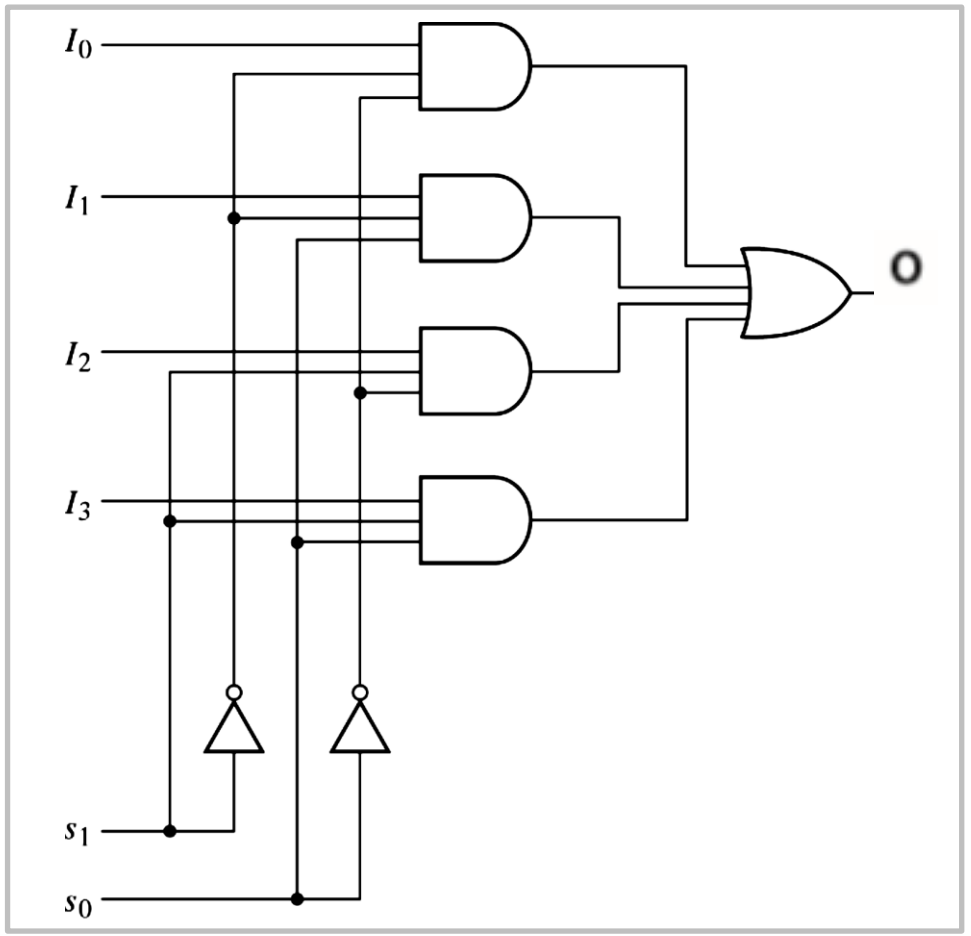
$$O = \overline{Sel}\, I_0 + Sel\, I_1$$

Multiplexers (MUX)

4-to-1 MUX

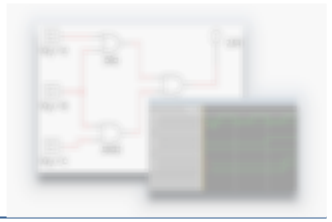


sel_1	sel_0	O
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$O = \overline{sel_1}\,\overline{sel_0}\,I_0 + \overline{sel_1}\,sel_0\,I_1 + sel_1\overline{sel_0}\,I_2 + sel_1\,sel_0\,I_3$$

Demultiplexers (DEMUX)



A **demultiplexer** is a combinational logic circuit that routes a single data input to one of several outputs.

- The selected output is determined by the binary value of the **select lines**.
- A standard DEMUX with **s select lines** has **2^s data outputs**.
- In an active-high DEMUX, the selected output follows the data input, while all non-selected outputs remain at logic 0.

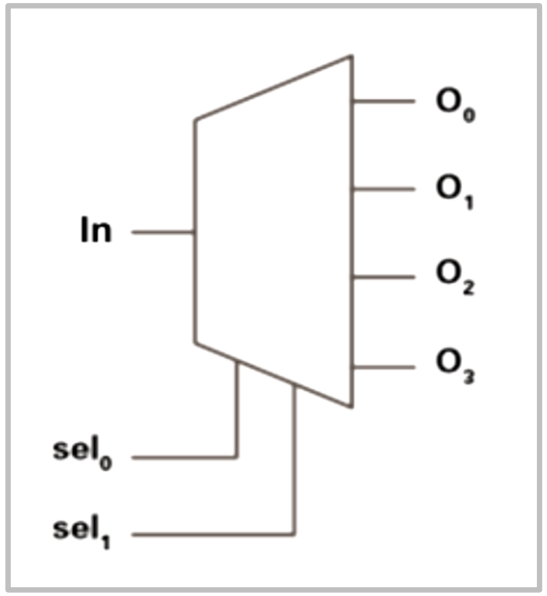
  For example: 1-to-4 DEMUX: 2 select line
  1-to-8 DEMUX: 3 select lines

- Common applications: Data routing and distribution
  Communication systems
  Serial-to-parallel data distribution
  Selection of destination devices or channels

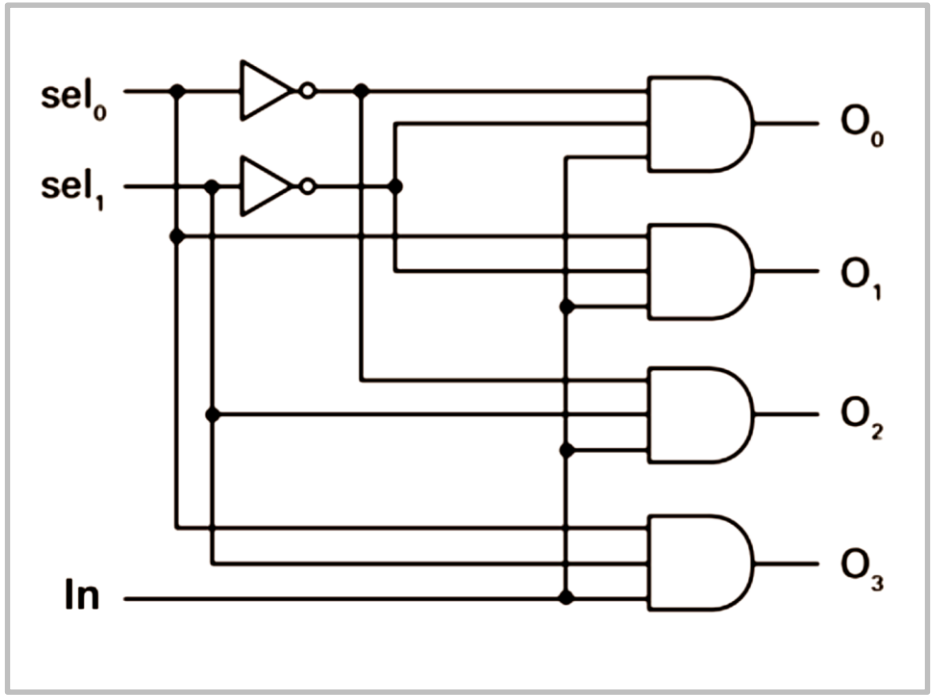
Demultiplexers (DEMUX)

- The graphical symbol for a 1-to-4 demultiplexer is shown below (left) as well as the corresponding 1-to-4 DEMUX truth table (center) and the gate-level implementation (right).
- The selected output follows the data input, while all other outputs remain LOW.

1-to-4 DEMUX



sel_1	sel_0	O_3	O_2	O_1	O_0
0	0	0	0	0	In
0	1	0	0	In	0
1	0	0	In	0	0
1	1	In	0	0	0



$$O_0 = In\ \overline{sel_1}\ \overline{sel_0}$$

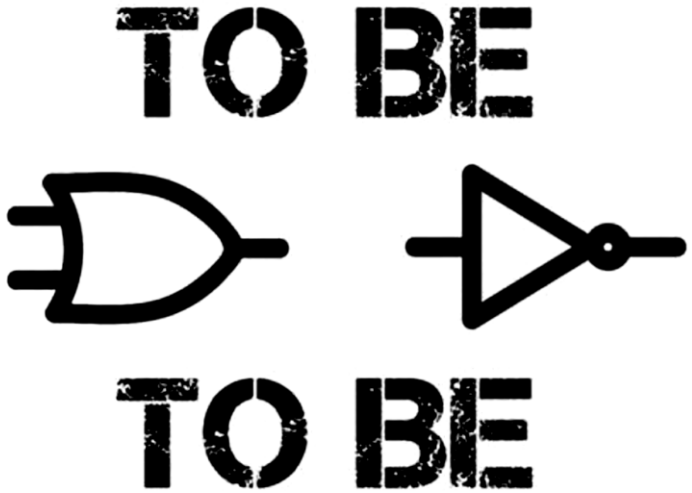
$$O_1 = In\ \overline{sel_1}\ sel_0$$

$$O_2 = In\ sel_1\overline{sel_0}$$

$$O_3 = In\ sel_1\ sel_0$$

Ευχαριστώ για την προσοχή σας!

- **Ερωτήσεις / Απορίες ;**



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