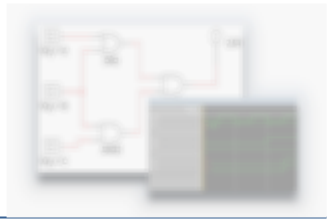


ECE119 – Ψηφιακή Σχεδίαση

Διδάσκοντες Εργαστηρίου: Δ. Καραμπερόπουλος
Α. Φεύγας
Μ. Πανταζή

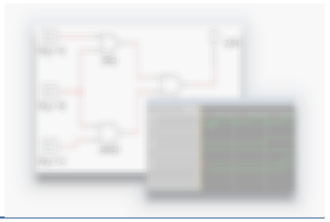
- Lab 6: Encoders and Decoders

Περιεχόμενα Εργαστηριακού Μαθήματος



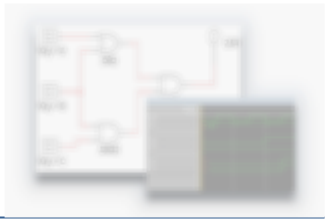
- Εισαγωγή
- Lab 1: Multisim Circuit Simulation and Basic Gates
- Lab 2: Truth Tables and Basic Logic Gates
- Lab 3: Logic Gates Explored and Boolean Algebra
- Lab 4: Karnaugh Maps
- Lab 5: Binary Conversion and Adders
- **Lab 6: Encoders and Decoders**
- Lab 7: Multiplexers and Demultiplexers
- Lab 8: Latches and Sequential Logic Circuits
- Lab 9: Flip-Flops
- Lab 10: Sequential Circuits – FSM (1ο)
- Lab 11: Sequential Circuits – FSM (2ο)

Encoders and Decoders



- In Lab 5, we learned that gates arranged to perform a specific function, such as binary addition, can be represented with a chip.
- Other applications of this concept include encoders and decoders.
- **Encoders** convert information from multiple input lines into a compact binary code.
  - Π.χ. **Encoder 4-to-2**: τέσσερις γραμμές εισόδου → δυαδικός κώδικας 2 bits.
- **Decoders** interpret binary codes to activate specific outputs or control devices.
  - Π.χ. **Decoder 2-to-4**: δυαδικός κώδικας 2 bits → μία από τέσσερις γραμμές εξόδου.
- In a previous lab, we learned what a seven-segment display is and in this lab we will explore how decoders apply to this electronic device.

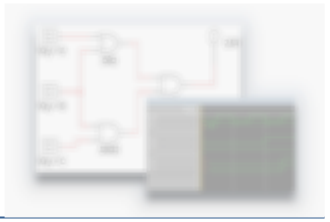
Learning Objectives



In this lab, students will:

- Explain the operation of binary encoders and decoders.
- Distinguish between standard and priority encoders.
- Understand the role of enable signals and active-high/active-low logic.
- Explain how a BCD-to-seven-segment decoder controls a display.
- Build and simulate a BCD-to-seven-segment decoder circuit and verify its operation.

Expected Deliverables

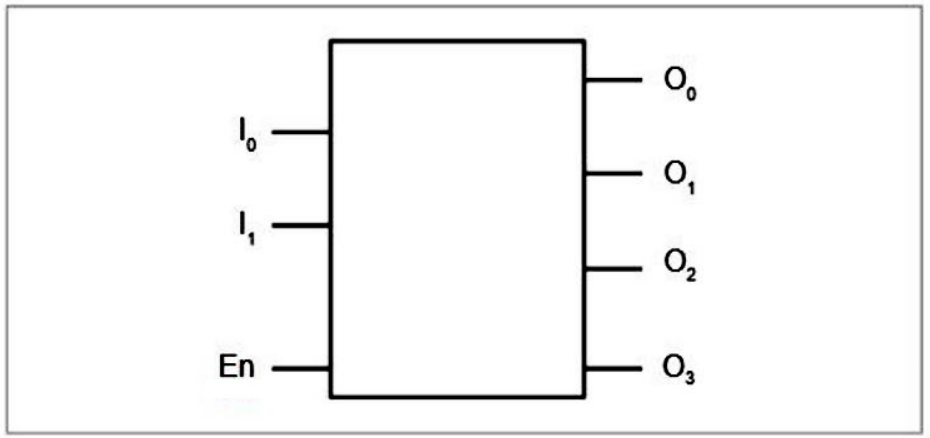


In this lab, you will collect the following deliverables:

- Diagram of a BCD to 7 Segment Display Decoder
- Truth tables
- Conclusion questions
- Verilog decoder implementation
- Testbench
- Simulation waveforms.

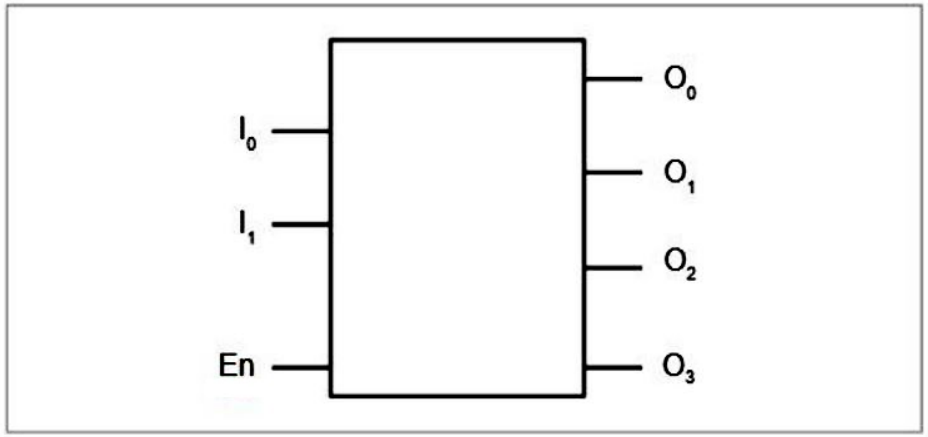
Decoders

- A **decoder** is a combinational logic circuit that converts an n-bit binary input into a specific output pattern. In a standard binary n-to-2^n decoder, exactly one output is activated for each input combination when the circuit is enabled.

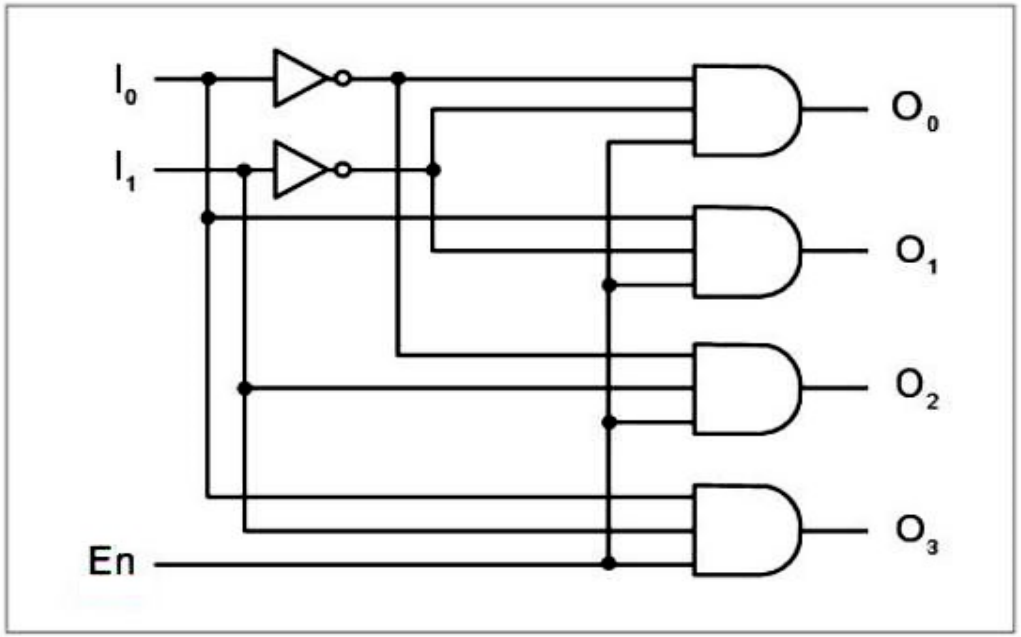


Decoders

- Let's take the example of a **2 to 4 decoder** enabled when the En signal is 1 (active-high):



En	I_1	I_0	O_3	O_2	O_1	O_0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0
0	x	x	0	0	0	0



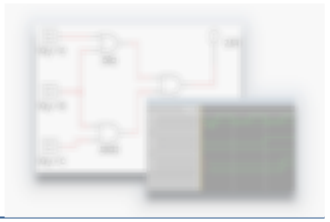
$$O_0 = En\,\overline{I_1}\,\overline{I_0}$$

$$O_1 = En\,\overline{I_1}\,I_0$$

$$O_2 = En\,I_1\,\overline{I_0}$$

$$O_3 = En\,I_1\,I_0$$

Decoders

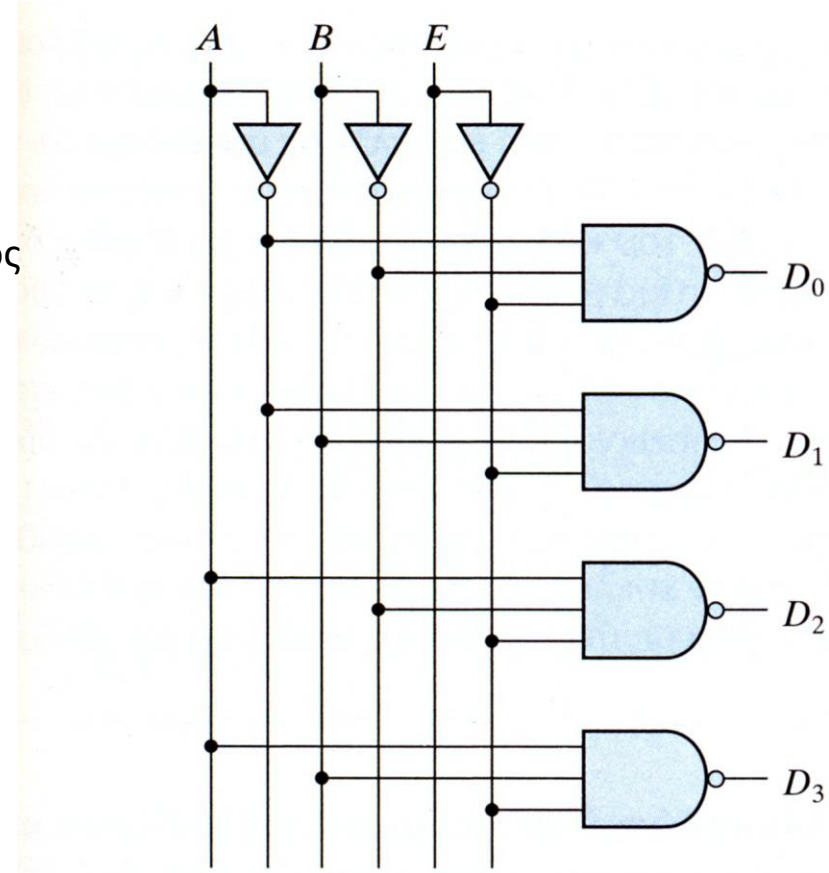


- **Decoders** take binary codes of n bits and have 2^n outputs.
- The outputs of an active-high binary decoder are **one-hot encoded** when the circuit is enabled, since exactly one output is 1 for each input combination.
- Decoders can include an **enable signal** for controlling the circuit operation.
- This enable signal can be **active-low** (meaning that the circuit will operate only when enable is 0) or **active-high** (the decoder is enabled when enable is 1).
- Decoders with enable inputs can be used for constructing larger decoders.
- One of the most important applications of decoders is memory access, where they are used for decoding the address of the rows in the memory blocks.

Decoders - 2x4 line decoder with enable input

2 to 4 decoder

- **Active-low enable**: το κύκλωμα ενεργοποιείται όταν En=0.
- **Active-low outputs**: η επιλεγμένη έξοδος γίνεται 0 αντί για 1.

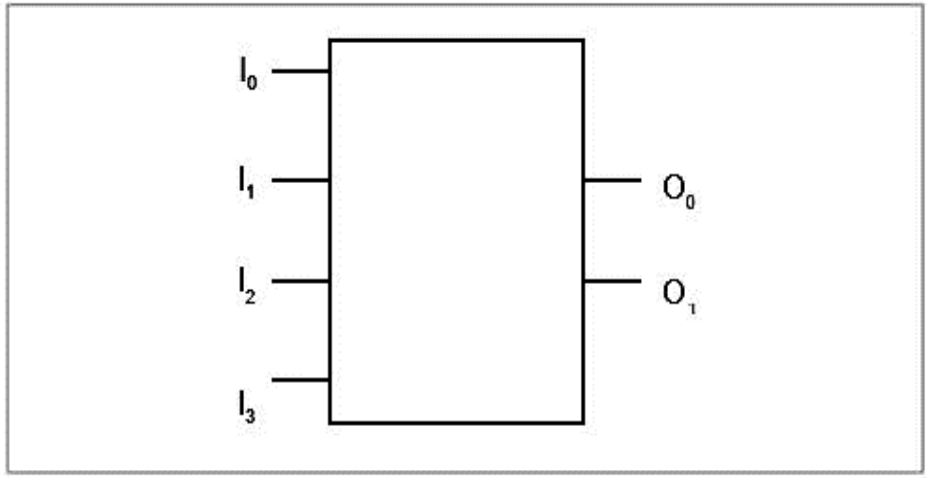


E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

ΣΧΗΜΑ 4.19
Αποκωδικοποιητής 2 × 4 με είσοδο επίτρεψης

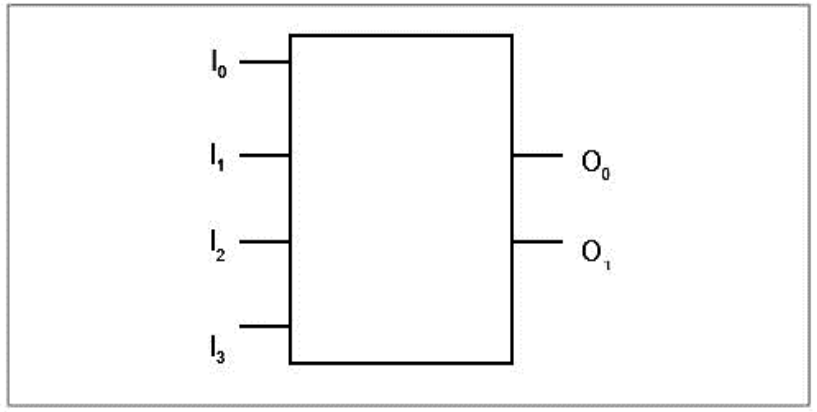
Encoders

- **Encoders** are logic circuits that perform the opposite function of a decoder.
- Binary encoders encode information from 2^n input lines, producing an n-bit code.



Encoders

- In a standard binary encoder, **only one input is assumed to be active at a time** (one-hot input).
- Encoding is used for reducing the number of bits needed to represent information. Encoders are commonly used in applications such as data transmission and storage.
- The graphical symbol of the **4 to 2 binary encoder** is presented below. The cases in which more than one input is 1 are not shown in the truth table because they are treated as don't care conditions (as we guarantee that they will not appear in normal operation).

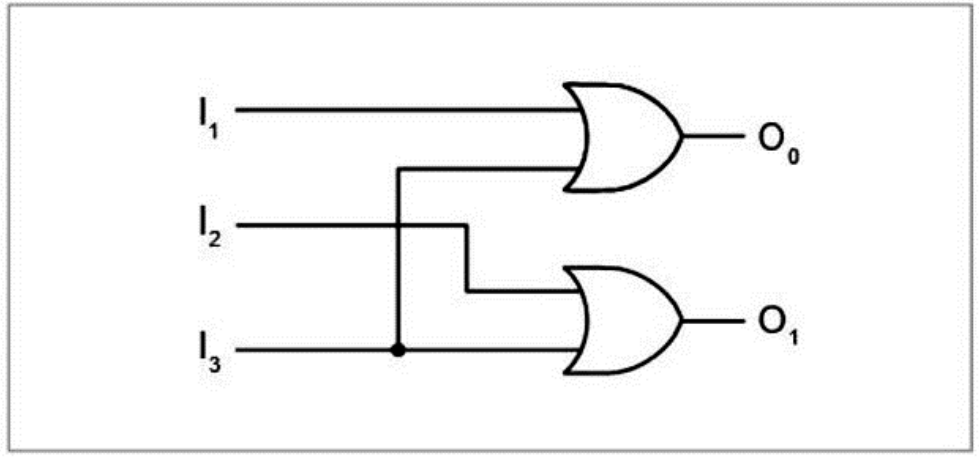


I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Encoders

- It can be seen in the truth table that the output O_1 **is 1** when either I_3 **or** I_2 **is 1** and that the output O_0 **is 1** when either I_3 **or** I_1 **is 1**.
- The input I_0 does not appear in the output equations, since its activation produces the binary code 00.
- The encoders presented so far are considered to have **one-hot encoded inputs**.

I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

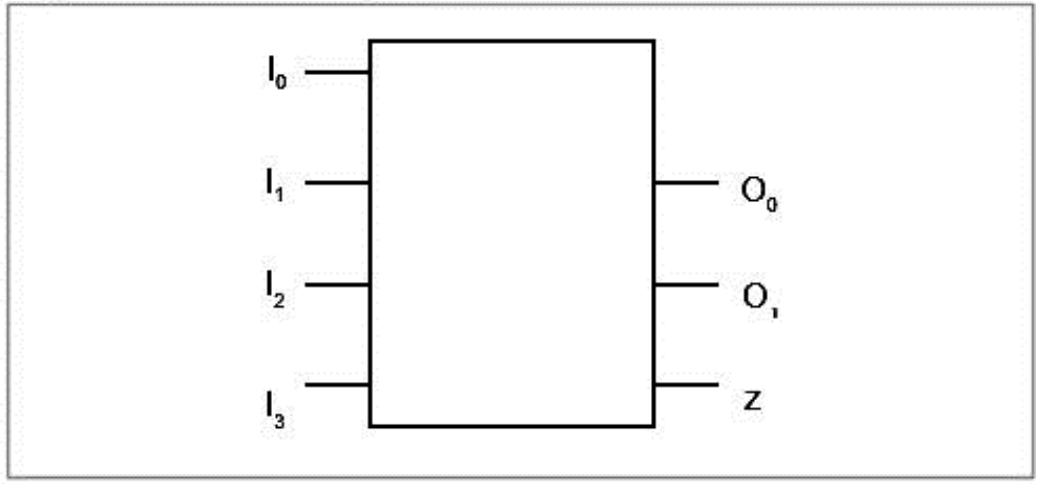


$$O_0 = I_1 + I_3$$

$$O_1 = I_2 + I_3$$

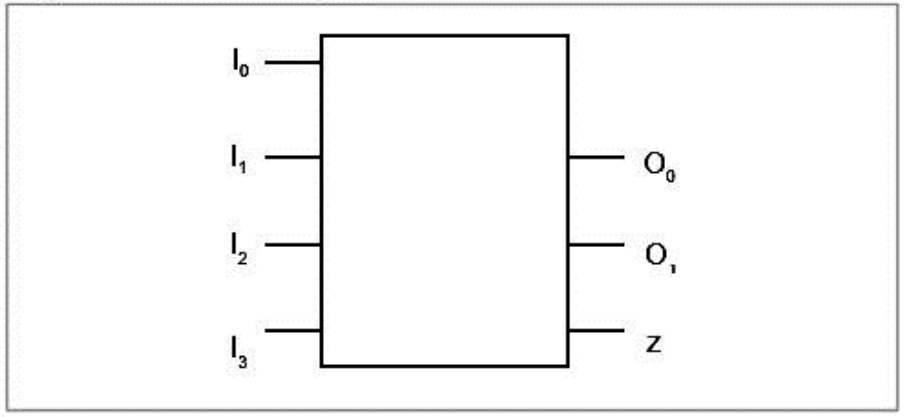
Priority encoders

- **Priority encoders** are able to prioritize inputs
- This is important because regular encoders can generate the wrong output when there is more than one input present at logic level 1.
- The priority encoder has an additional **output, z** (valid input indicator), which is 1 when at least one input is active and 0 when no input is active.



Priority encoders

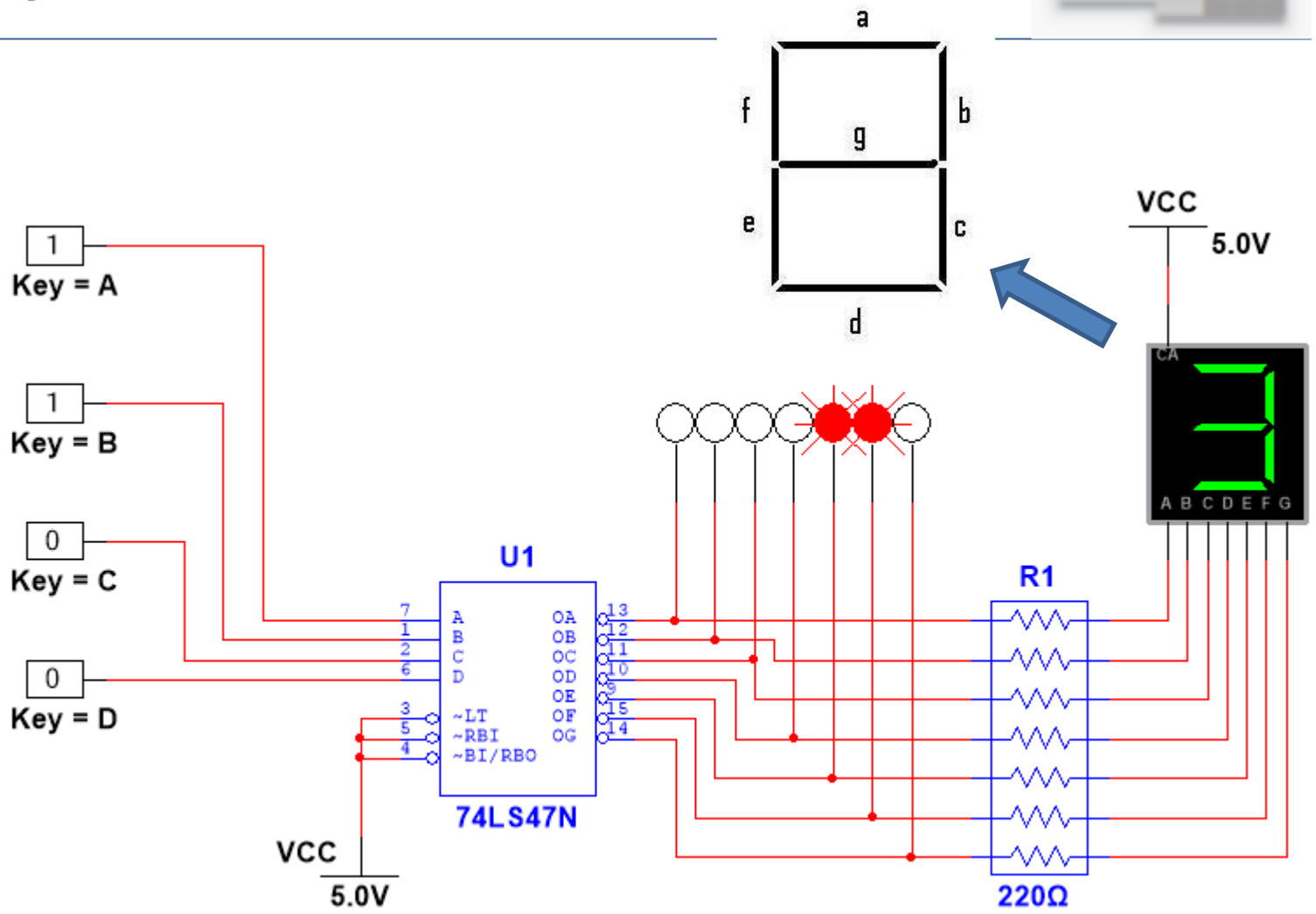
- The truth table describes the behavior of a **4-to-2 priority encoder**.
- It can be seen that: When I_3=1, the encoder produces O_1O_0=11 and z=1, regardless of the values of the lower-priority inputs.
- The priority is: $I_3 > I_2 > I_1 > I_0$
- For example, if I_3 =1 and I_1=1, the output is 11, because I_3 has higher priority.



I_3	I_2	I_1	I_0	O_1	O_0	z
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

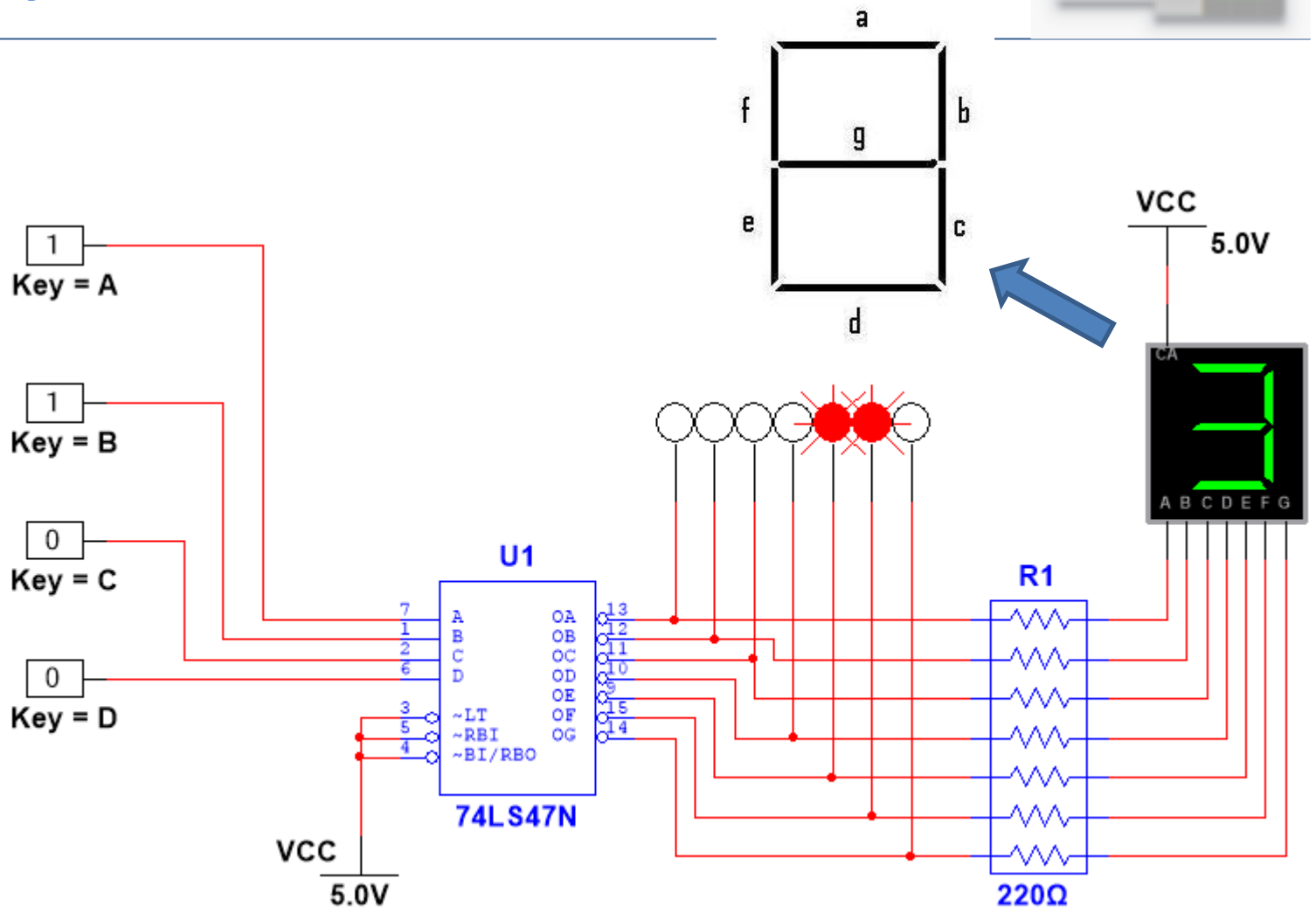
BCD to Seven Segment Display Decoder

- **BCD inputs** (A, B, C, D): Αναπαριστούν ένα δεκαδικό ψηφίο 0–9 με 4 bits.
- **Seven outputs** (a–g): Ελέγχουν ποια τμήματα της οθόνης θα φωτιστούν.
- **Active-low outputs**: Μια έξοδος LOW ενεργοποιεί το αντίστοιχο τμήμα.
- **Current-limiting resistors**: Οι αντιστάσεις περιορίζουν το ρεύμα στα LED της οθόνης.



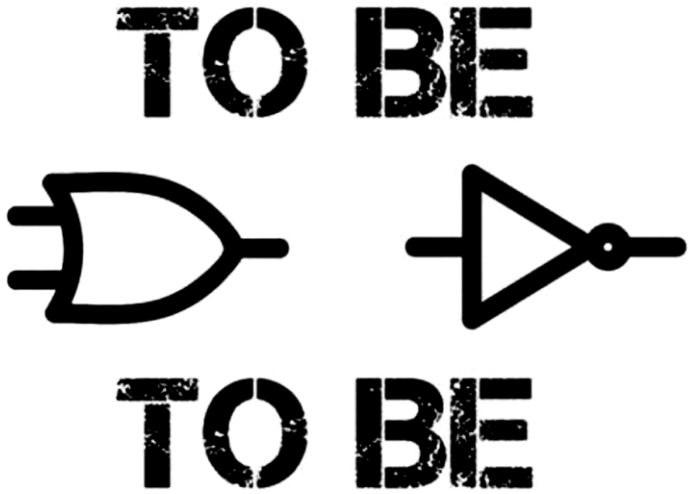
BCD to Seven Segment Display Decoder

- **Valid BCD inputs** range from 0000 to 1001 (decimal 0–9).
- The combinations 1010–1111 are not valid BCD digits.
- **Invalid BCD inputs** do not necessarily produce undefined outputs. The actual behavior depends on the decoder.



Ευχαριστώ για την προσοχή σας!

- **Ερωτήσεις / Απορίες ;**



Επικοινωνία: ece119.uth@gmail.com