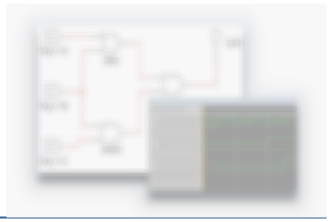


ECE119 – Ψηφιακή Σχεδίαση

Διδάσκοντες Εργαστηρίου: Δ. Καραμπερόπουλος
Α. Φεύγας

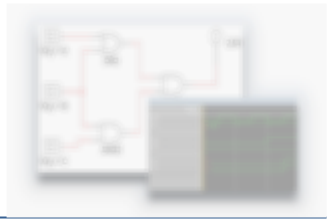
- Lab 2: Truth Tables and Basic Logic Gates

Προεπισκόπηση Εργαστηριακού Μαθήματος



- Εισαγωγή
- Lab 1: Multisim Circuit Simulation and Basic Gates
- **Lab 2: Truth Tables and Basic Logic Gates**
- Lab 3: Logic Gates Explored and Boolean Algebra
- Lab 4: Karnaugh Maps
- Lab 5: Binary Conversion and Adders
- Lab 6: Encoders and Decoders
- Lab 7: Multiplexers and Demultiplexers
- Lab 8: Latches and Sequential Logic Circuits
- Lab 9: Flip-Flops
- Lab 10: Sequential Circuits – FSM (1ο)
- Lab 11: Sequential Circuits – FSM (2ο)

Lab 2: Truth Tables and Basic Logic Gates



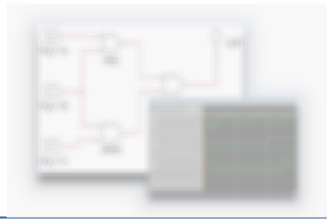
Nowadays, **digital hardware** is encountered in almost every aspect of our everyday life, being part of personal computers, household appliances, robots, television networks, etc.

Logic circuits are the building blocks of digital hardware.

The logic circuits perform operations on digital signals and are usually implemented as electronic circuits where the signal values are restricted to a few **discrete values**.
The most common are the **binary logic circuits**, where the only values are **0 and 1**.

Although multi-valued logic systems with three or more logic levels exist, binary logic dominates practical digital circuit design because it provides simpler implementation and greater noise immunity.

Lab 2: Truth Tables and Basic Logic Gates



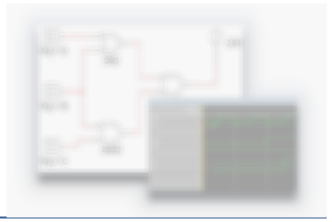
The three basic **logic operations** are:

- Logical **AND**
- Logical **OR**
- **NOT** operation (inversion)

The logic operations are implemented with **logic gates**.

A logic gate is an electronic circuit made up of **transistors**. The information related to the logic gates and logic functions and be described by a **truth table**.

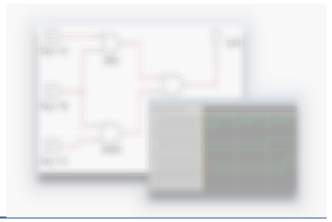
Learning Objectives



In this lab, students will:

- Explore the behavior of different configurations of logic gates.
- Configure and build circuits in Multisim.
- Learn basics in Verilog (HDL)

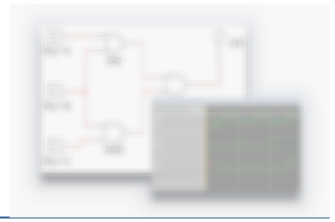
Expected Deliverables



In this lab, you will collect the following deliverables:

- Probe results
- True Tables
- Analysis of gate behavior
- Analysis of circuit behavior
- Circuit calculations
- Conclusion questions
- Multisim Files
- Verilog File

Truth Tables (1/4)



A common way to express the specific function of a logic circuit is the **truth table**.

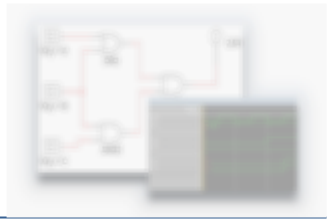
(*Other methods of presentation include Schematics, Boolean expressions, and Behavioral descriptions.)*

Truth tables show all permutations of the inputs with their corresponding output values in terms of logic level states.

Logic level states are typically expressed as:

- 1 and 0
- HIGH and LOW
- True and False

Truth Tables (2/4)



This is an example of a truth table for two inputs:

A	B	Out
0	0	0
0	1	1
1	0	0
1	1	1

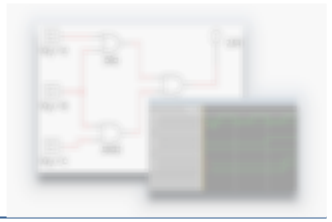
Truth Tables (3/4)



A gate or logic circuit's truth table must have as many rows as there are possibilities of unique input combinations.

- For a **single-input gate**, like the inverter, there are only two input possibilities, namely 0 and 1.
- For a **two-input gate** there are four possibilities (00, 01, 10, and 11), and thus four rows for the corresponding truth table.
- For a **three-input** logic device, there are eight possibilities and so forth. The input columns are typically written in binary order.

Truth Tables (4/4)



This is an example of a truth table for three inputs:

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Logic Gates (AND)

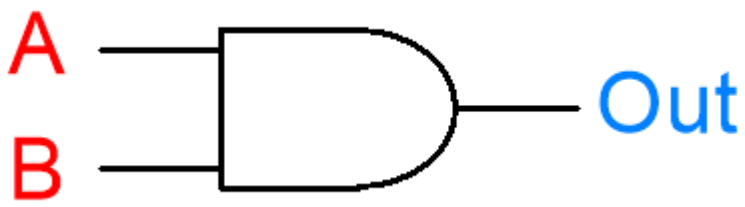
Logic gates are physical devices that implement the Boolean functions of truth tables.

The three most basic logic gates are the "**AND**", "**OR**" and "**NOT**".

- In the "**AND**" logic gate, the output is 1 if both the inputs for A and B are also 1. If one or all of the inputs for A and B are 0, then the resulting output is 0.

  *(Generally, the "AND" logic gate outputs the **minimum** value between the two input digits.)*

A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

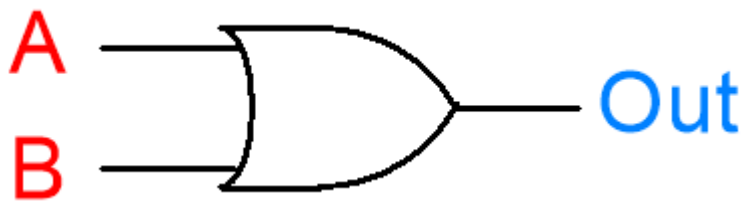


Logic Gates (OR)

- In the "**OR**" logic gate, the output is 0 if both the inputs for A and B are also 0. If one or all of the inputs for A and B are 1, then the resulting output is also 1.

  *(The "OR" logic gate outputs the **maximum** value between the two input digits.)*

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1

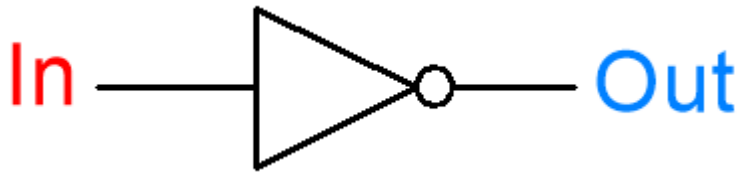


Logic Gates (NOT)



- The “**NOT**” logic gate is also known as **Inverter**.
- It has only one input and one output.
- The truth table for an inverter is simple. The output is always the opposite of the input.
- For example, if the input is 1, the output will be 0 and vice versa. Visually this is depicted by a circle at the input and/or output ends of the logic gates.
- In this situation, the circle is at the output, which means that the output is inverted. If it was at the input, then it is the input that would be inverted.

In	Out
0	1
1	0



Άσκηση: Θεώρημα 1



Με μια πύλη OR 2 εισόδων επιβεβαιώστε το θεώρημα της άλγεβρας Boole σύμφωνα με το οποίο ισχύει η ακόλουθη σχέση: **x + x = x**. Συμπληρώστε τον κατάλληλο πίνακα αληθείας, αναγράφοντας όλους τους πιθανούς συνδυασμούς τιμών.

Η προσομοίωση να γίνει με το Multisim.



Όνομα αρχείου: “2_Theorem_1.ms14”

Άσκηση: Θεώρημα 3, Διπλή άρνηση



Τοποθετείστε και συνδέστε σε σειρά δύο αντιστροφείς και επιβεβαιώστε το θεώρημα της Άλγεβρας Boole: **(x')' = x**. Συμπληρώστε τον κατάλληλο πίνακα αληθείας, αναγράφοντας όλους τους πιθανούς συνδυασμούς τιμών.

Η προσομοίωση να γίνει με το Multisim.



Όνομα αρχείου: “2_Theorem_3.ms14”

Άσκηση: Θεώρημα 6, Απορρόφησης



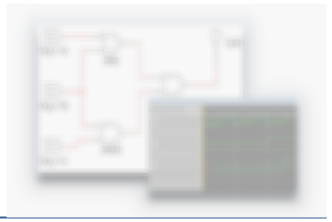
Χρησιμοποιώντας τα κατάλληλα κυκλωματικά στοιχεία επιβεβαιώστε το θεώρημα απορρόφησης κατά το οποίο ισχύει η ακόλουθη σχέση: **x + xy = x**. Συμπληρώστε τον κατάλληλο πίνακα αληθείας, αναγράφοντας όλους τους πιθανούς συνδυασμούς τιμών.

Η προσομοίωση να γίνει με το Multisim.



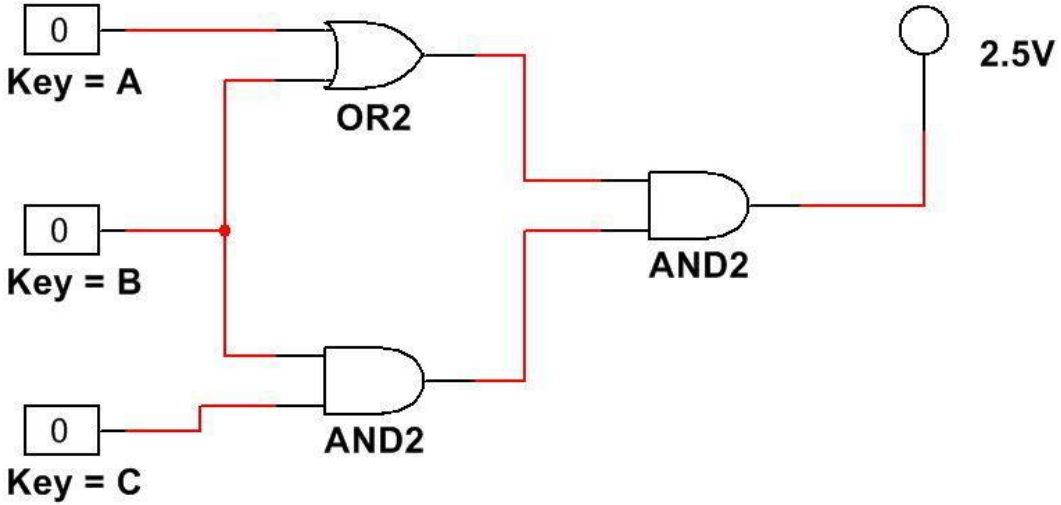
Όνομα αρχείου: “2_Theorem_6.ms14”

Simulate: Building a Circuit with Multiple Gates (1/2)

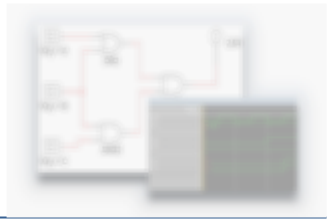


Build the following circuit using multiple AND/OR Gates in Multisim:

- Place an **OR** gate and two **AND** gates from the Misc Digital group.
- Place three **INTERACTIVE_DIGITAL_CONSTANTs** from the Sources group.
- Place one **PROBE_DIG_RED** from the Indicators group.
- Wire them as shown.



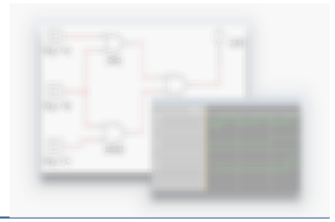
Simulate: Building a Circuit with Multiple Gates (2/2)



- Click the **Run** button to begin simulating the circuit.
- Using the **A**, **B**, and **C keys**, vary the inputs into the circuit.
- Record the results, as indicated by the probe, in the following truth table.

A	B	C	Out
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

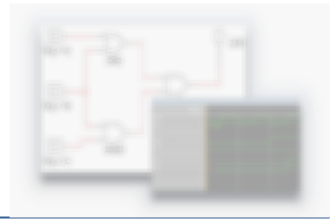
Exercise: Determining a Circuit from a Truth Table (1/2)



- In this part, you'll look at a few simple truth tables and determine their circuits.
- Given the following truth table, determine which configuration of gates would give you these results.
- You can:
  - Use trial and error simulation in Multisim
  - Calculate different circuits on paper
  - Use whatever other methods you find useful
  - **Use gates with 1 or 2 inputs**

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Exercise: Determining a Circuit from a Truth Table (2/2)



- Given the following truth table, determine which configuration of gates would give you these results.
- You can:
  - Use trial and error simulation in Multisim.
  - Calculate different circuits on paper.
  - Use whatever other methods you find useful
  - **Use gates with 1 or 2 inputs**

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Exercise: Γλώσσα Περιγραφής Υλικού HDL - Verilog

Γράψτε την περιγραφή HDL σε επίπεδο πυλών του παρακάτω κυκλώματος “Figure 2.10”.

Μεταγλωττίστε τον κώδικά σας με την χρήση του Icarus.



Όνομα αρχείου “Figure2_10.v”.

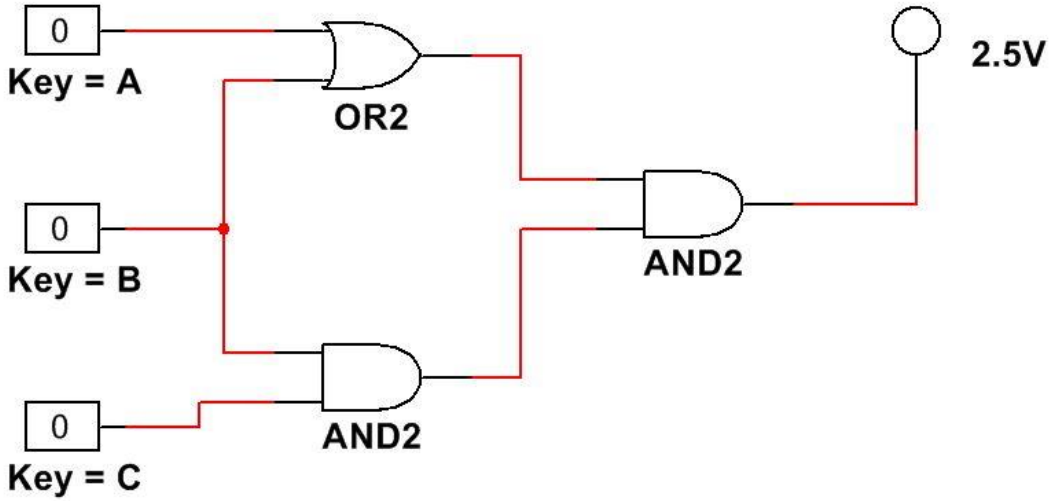
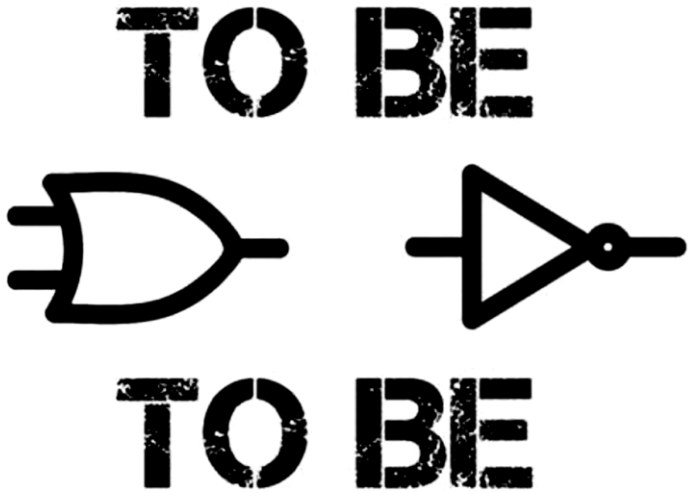


Figure 2-10 Circuit with AND, OR Logic gates

Ευχαριστώ για την προσοχή σας!

- **Ερωτήσεις / Απορίες ;**



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